

Works and Plans (what I have done and what I will do)

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What is B-Factory?



KEKB Accelerator + Belle Detector



Physics @ Belle



Silicon Vertex Detector

over 20 institutes ~100 members

Belle Detector



SVD1 (upto 2003 summer)	SVD2 (upto now)
3-layer (R3rd = 6.0cm)	4-layer (R4th = 8.8cm) better low P tracking
2.0 (3.0) cm radius	1.5 (2.0) cm radius better vertex
of beam pipe (1st lyr)	of beam pipe (1st lyr) resolution
23°< θ < 139°	$17^{\circ} < \theta < 150^{\circ}$ larger acceptance
VA1 (0.8 μ m) : < 1MRad	VA1TA (0.35 μ m) : < 20MRad rad. hard

Activities in SVD

1996 ~

for Belle (esp. software) .SVD Simulation (SVD1.0, 1.2, 1.4, 1.6, 2.0) . Offline data format (SVD1 \rightarrow SVD2) . Clustering (w/ T.Hojo@Osaka) . Tracking (w/K.Trabelsi@KEK) . trigger simulation . SVD2.0 design . Alignment . Data quality monitor . SVD3 simulation / reconstruction / physics test / design ... for Super-Belle . New readout chip test (w/ T.Tsuboyama+T.Kawasaki)

. modification of Geant3-base simulation

. beam background study (simulation / single-beam run data)

SVD3 was not installed finally.

Configuration Design Beam Pipe Design

Beam background components

. Particle (Beam-gas, Touschek, ...) . SR (direct / backscattering)

Hurdles faced by VTX detector . High radiation (several MRad/yr: CM05/S01 tech.)

. High occupancy

increases fake clusters degrades tracking performance deteriorates vertex resolution

→ have to reduce BG hits as much as possible Behavior of low-E γ (<100keV) is very important !! PXD Occupancy

Single beam run (beam





Activities in Belle

1996 ~ for Belle (esp. software) . management of Geant3-based Simulation (not only for SVD) . implementaion of run-dependence . beam background overlay scheme . W/o this, nobody can make realistic MC data . effect of higher beam background . estimation of the tracking eff. in Hadron event (CDC, KLM) . MC mass production for Super-Belle . Geant3-base simulation for Study Report (ECL, ACC, CDC, SVD,...)

. geometrical design, BG effect, material budget tracking part of the fast simulator for physics studies . manage and develop Geant4-base simulation for TDR

Super-Belle in Geant4

Tracking + Vertexing



Activities in Belle

1996 ~ Physics analyses . CPV with $B \rightarrow \chi_{c1}$ Ks (w/ D.Heffernan) $B \rightarrow \tau \nu$ (2002 \rightarrow lkado@Nagoya in 2006) $.B \rightarrow \phi \pi$ (2006 \rightarrow a Korean student) Belle Software Festa 2007 - Windows Internet Explorer Education 🙆 http://belle.kek.jp/~harat/software2007/Festa-top.html くここからJWord検索 👻 🍫 🗙 Live Search 2 ファイル(F) 編集(E) 表示(V) お気に入り(A) ツール(T) ヘルプ(H) 💌 検索 🗤 🧭 💕 👻 📩 ブックマークマ 👰 ブロック数: 0 🖤 チェック マ 🍙 次に送信マ 🍐 . Software Festa in 2007 設定
🐴 🔹 🔝 🔹 📥 🔹 🞲 ページ(P) 🖛 🍈 ツール(O) 🖛 Belle Software Festa 2007 It is important to encourage young students to increase the number of publications from Belle BELLE Software Festa '07 date/place program contacts participants volunteers requirement Gallery **Belle** Tour QuickFesta

My works are like ...



My works are like ...



My works are like ...

Super Belle

Without Atlas ...

KEK Roadmap



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Super Belle Detector



Plans for Super-Belle

We have only a couple of years !!

SVD+PXD

. management of Geant4-based Simulation (not only for SVD)

. reconstruction software (clustering, tracking) esp. PXD+SVD self-tracking is very important for physics . low-P tracking cannot be done in CDC

- . impact on CPV in D*D*, etc...
- . impact on full-reconstruction event

. feedback on hardware design from physics requirement check the hardware-oriented design

. chip-on-sensor

. detector configuration

. systematic error caused by mis-alignment

. decision of the readout chip and pixel technology . full demonstration of APV25 front-end, repeater, FADC . DEPFET/CMOS/SOI

Chip-on-Sensor



Technology options

	DEPFET	CMOS (CAPS/MAPS)	501
Material budget	20 ~ 100µm (adjustable)	<~50 μ m (sensitive area 5~10 μ m)	50~100 μm (could be <~50 μ m)
Size	limited by wafer (50 x 75 mm ²)	limited by reticle (21 x 21 mm ²)	limited by reticle (21 x 21 mm ²)
Power consumption	small (0.5w) (reset switcher chip: Voltage swing > 8V)	small	small
Radhardness (3MRad/yr?)	tested < 1MRad (up to 8MRad?: irradiation test)	intrinsic rad. hard (must be > 30MRad)	tested > 30MRad
10kHz trig. rate	estimated ~1% ineff.	? (CAP3 too slow)	not proved
Availability	MPI only (already used in other exp.)	R&D in progress	R&D in progress

Plans for Super-Belle

Current Problems . less communication . unplanned update . human resource

need

a "head"

We have only a couple of years !! Super-Belle management of software . reconstruction tools . vertexing (PXD, SVD) . tracking (PXD, SVD, CDC) . PID (CDC, A-RICH, TOP, ECL, KLM) . GEANT4-base simulation (required for TDR) . analysis tools . tag-side vertexing, etc... . software framework (BASF, Marlin, etc ...) . Improvement of hermeticity . important for $B \rightarrow \tau \nu$, $K \nu \nu$

. beam background study

. feedback on the IR design . check the occupancy of the PXD/SVD

Plans for Super-Belle





Backup



Activities in Kamioka



Physics Results



Beam Pipe Design



DEPFET

Intense R&D has been done for ILC pixel sensors has been used in several experiments already! . Technology is available in MPI only . Sensor size is limited by wafer size $50 \,\mu\text{m} \times 75 \,\mu\text{m} : 215 \times 512$ pixel (adjustable) almost no gap in the acceptance . Not very rad-hard (tested up to 1Mrad) OK up to 8Mrad?? . Small power consumption . Reset switcher chip: Voltage swing > 8V . Thickness $20\mu m \sim 100\mu m$ (adjustable for experiments) . Doubly-correlated sampling can be done \rightarrow low noise . 10kHz trigger rate, O-suppression, ~4pixels/hit, 32 bits/pixel includiing address Disadvantage: ~1% inefficiency . Data processing is done in subsequent chips on repeater system or in backend system



CMOS pixel (CAPS/MAPS)

. The same technology as commercial CMOS cameras 5-10M -pixel chips are in production . Sensor size is limited by reticle size $(21 \times 21 \text{ mm}^2)$ $22.5 \,\mu m \, x \, 22.5 \,\mu m$ gap in the acceptance . Intrinsic rad-hard (deep sub-micron technology) > 30 MRad Particle . Sensor is a thin epitaxial layer (5~10 μ m thick) signal si small \rightarrow No problem as the detector capacitance is also small <= 50µm . N-well is used to collect charge from the epitaxial layer . 100kHz frame rate is achieved (132 x 48 pixel) Full-size detector (928 x 128 pixel) 10kHz trigger rate ???



SOI

. Activity started as PMOS NMOS one of KEK detector R&D project in 2005 Si02 BOX(Buried Oxide) D+Sensor size is limited by reticle size $(21 \times 21 \text{ mm}^{1+2})$ $20\mu m \times 20\mu m : 128 \times 128$ Sensor gap in the acceptance (High Resistive . rad-hard (deep 0.2 μ m technology) n-Substrate) tested > 30 MRad X-ray . Depletion depth of 50-100 μ m has been achieved thinning after silicon process $<=50\mu m$. Signal induced in the sensor can be processed by the CMOS circuit Complex/rad-hard circuit can be made DEPFET/CAP type readoout is also possible 10kHz trigger rate ??? . R&D in progress Evaluation of Belle PIXEL chip will start soon (pixel-shaper-discrimination-digital pipeline)

