

Kuno and Yamanaka Group Year-End Presentation 2017

Development of readout test system for prototype ASIC of pixel detector for ATLAS upgrade

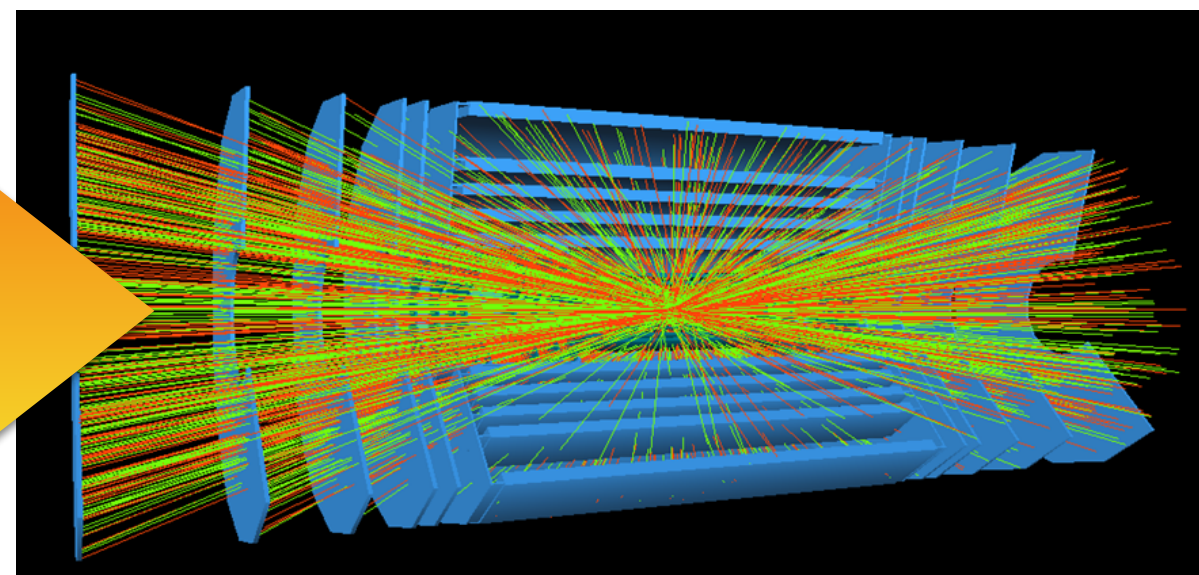
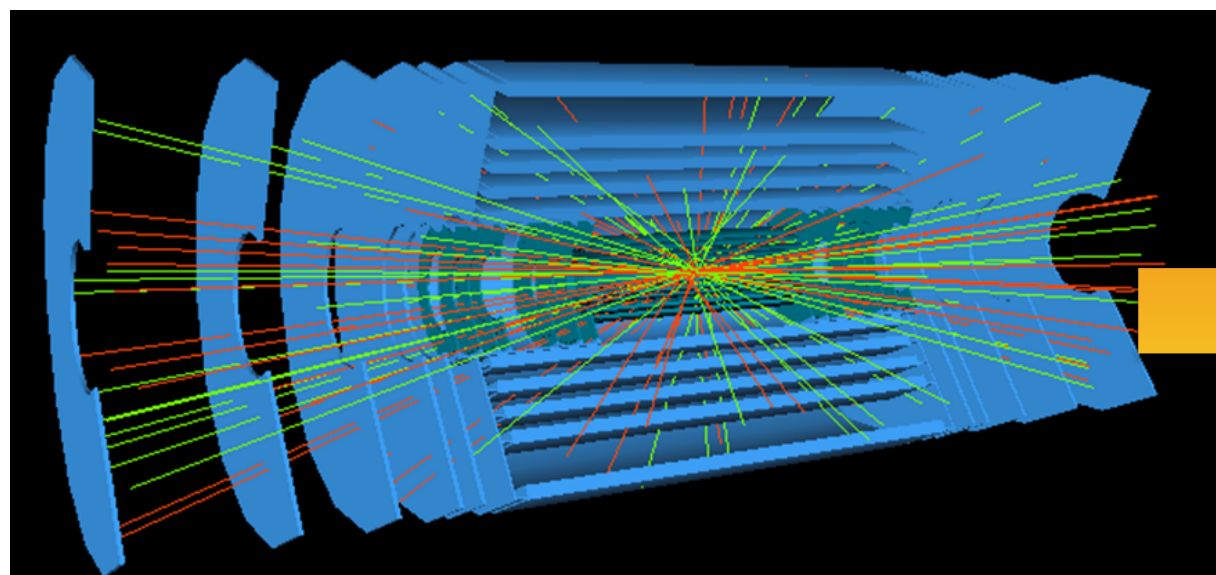
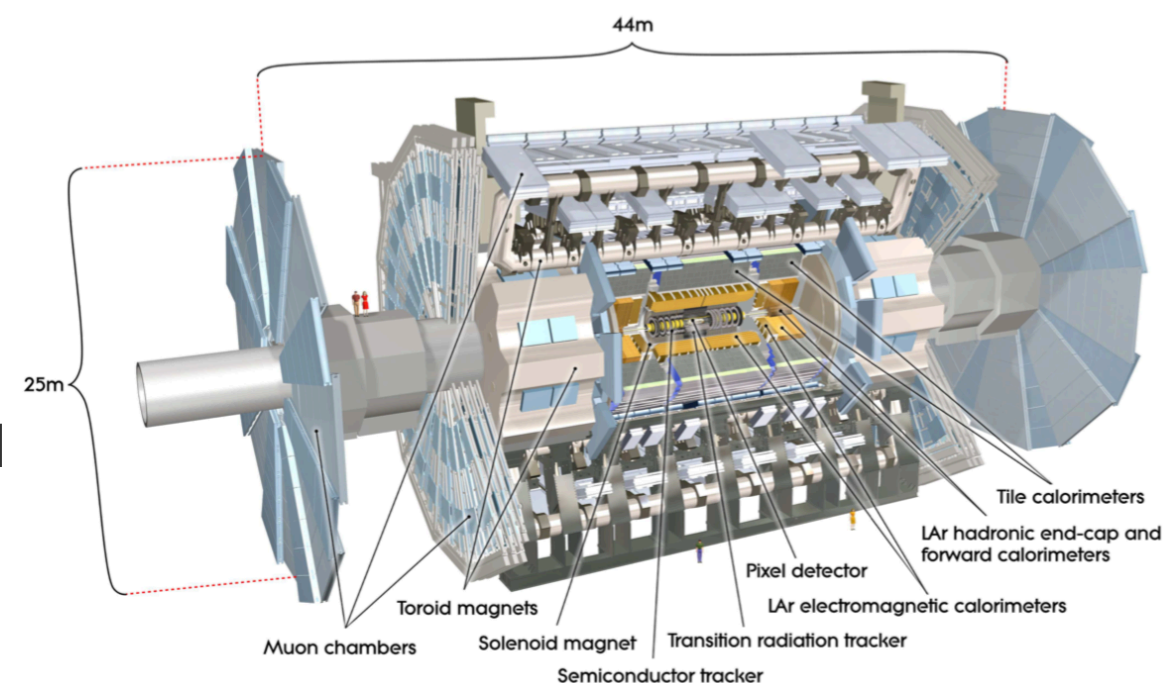
ATLASアップグレード用ピクセル検出器の
プロトタイプASIC読み出し試験システムの開発

28/12/2017
Osaka University
M2 Yasunori Sawada

- 1. ATLAS Experiment**
- 2. HL-LHC ATLAS Pixel**
- 3. Pixel ASIC**
- 4. ASIC Readout system**
- 5. Summary**

1. ATLAS Experiment - HL-LHC

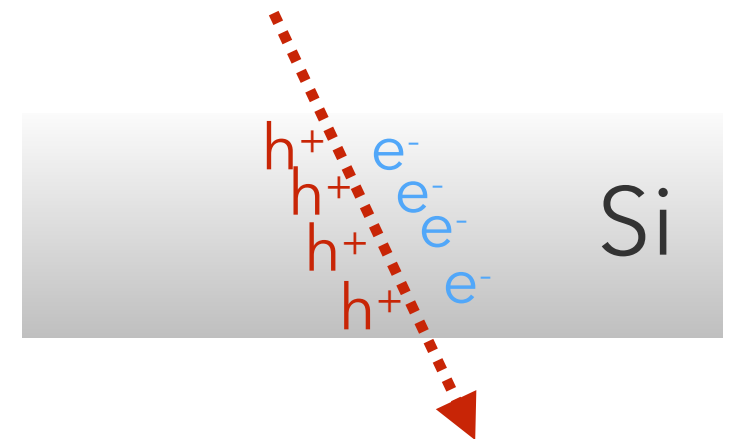
- HL-LHC ATLAS - 2026~
 - Energy - 14 TeV
 - Luminosity - $\sim 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$



2. HL-LHC ATLAS Pixel detector

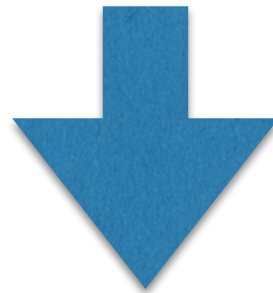
Semiconductor Sensor

Detect charged particles



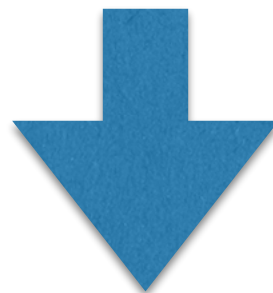
ASIC

(Application specific integrated circuit)



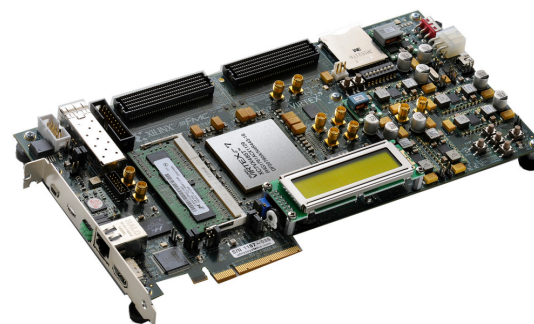
011101101111....

Digitization of signal
& some functions



FPGA Board

(Field programmable gate array)



Data processing,
PC Interface ...etc

2. HL-LHC ATLAS Pixel detector

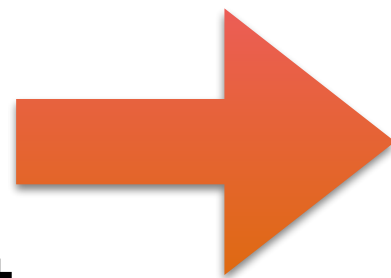
- *Pixel hit rate in HL-LHC ~ average 100-150*
- *Requirements*
 - Matrix size : 400×384
 - Pixel pitch : 50×50μm²
 - Trigger rate :
1 MHz (w/ <35μs latency)

~100 Hits/event × 1 MHz × 26 bit/Hit → ~2.6 Gbps

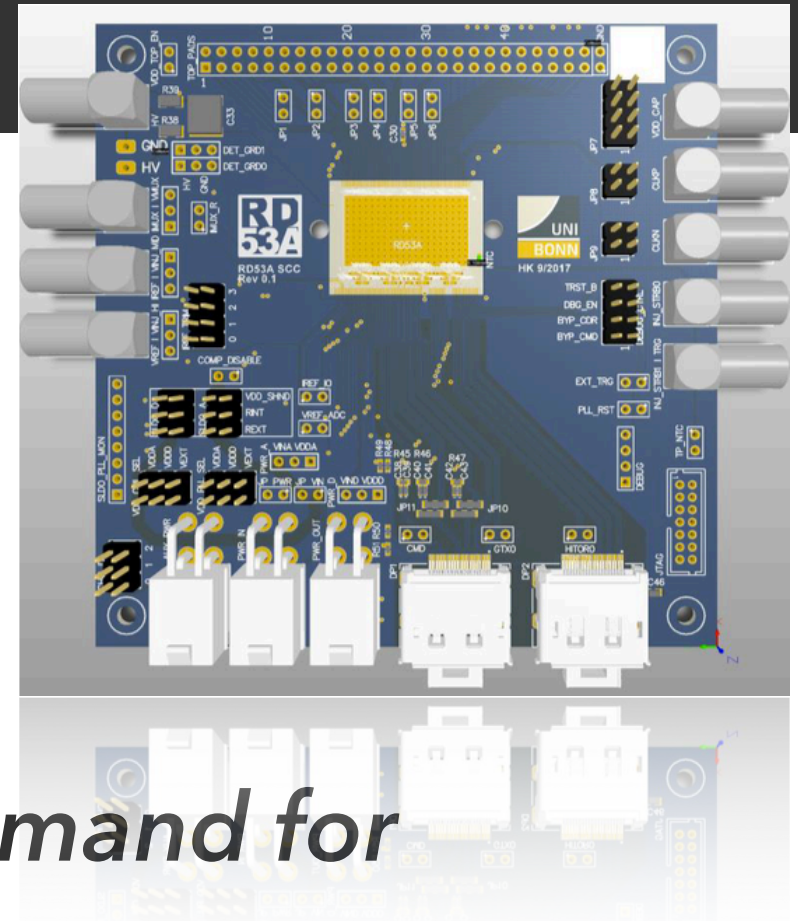
→ *Development ASIC, RD53 Collaboration*

3. Pixel ASIC - RD53A

- Prototype ASIC **RD53A**
 - Half size of production
- ATLAS Japan group
 - Radiation tolerance test
 - Test beam



***Demand for
Data acquisition system
development !***



- Required performance
 - Readout bandwidth : ~5 Gbps/chip

4.ASIC Readout System

Development milestones

- 1. **FE-I4** Readout system using **Ethernet**
- 2. **FE-I4** Readout system using **PCI Express**
 - **FE-I4** - Currently used **ASIC** in **ATLAS Pixel**
- 3. **RD53A** Readout system using **PCI Express**



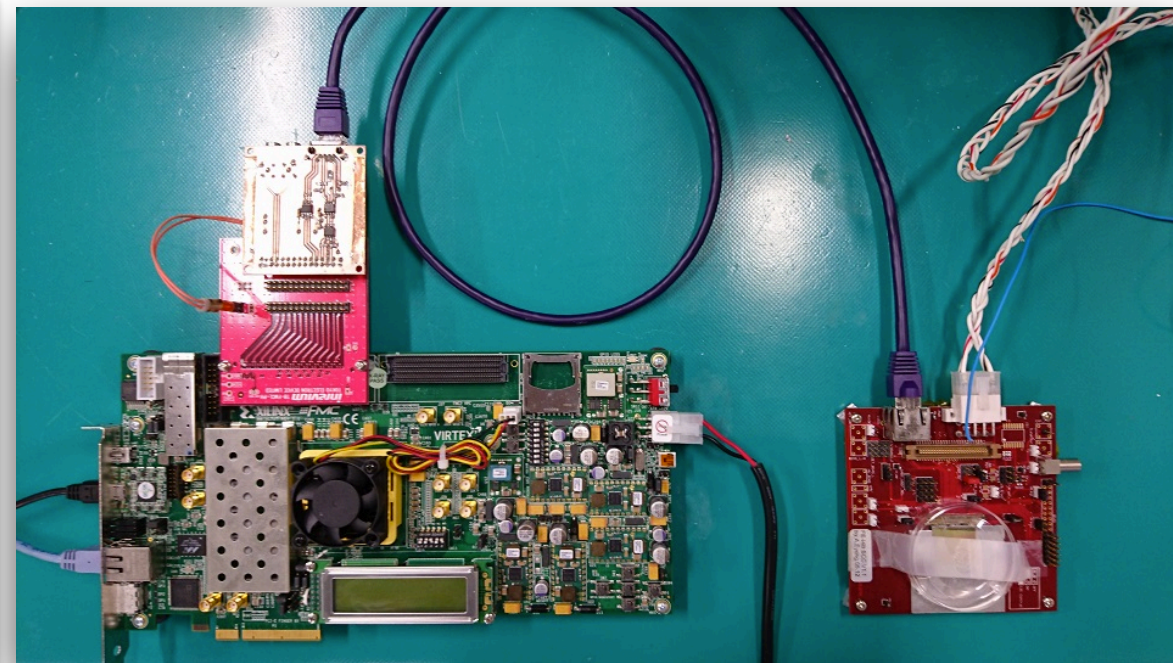
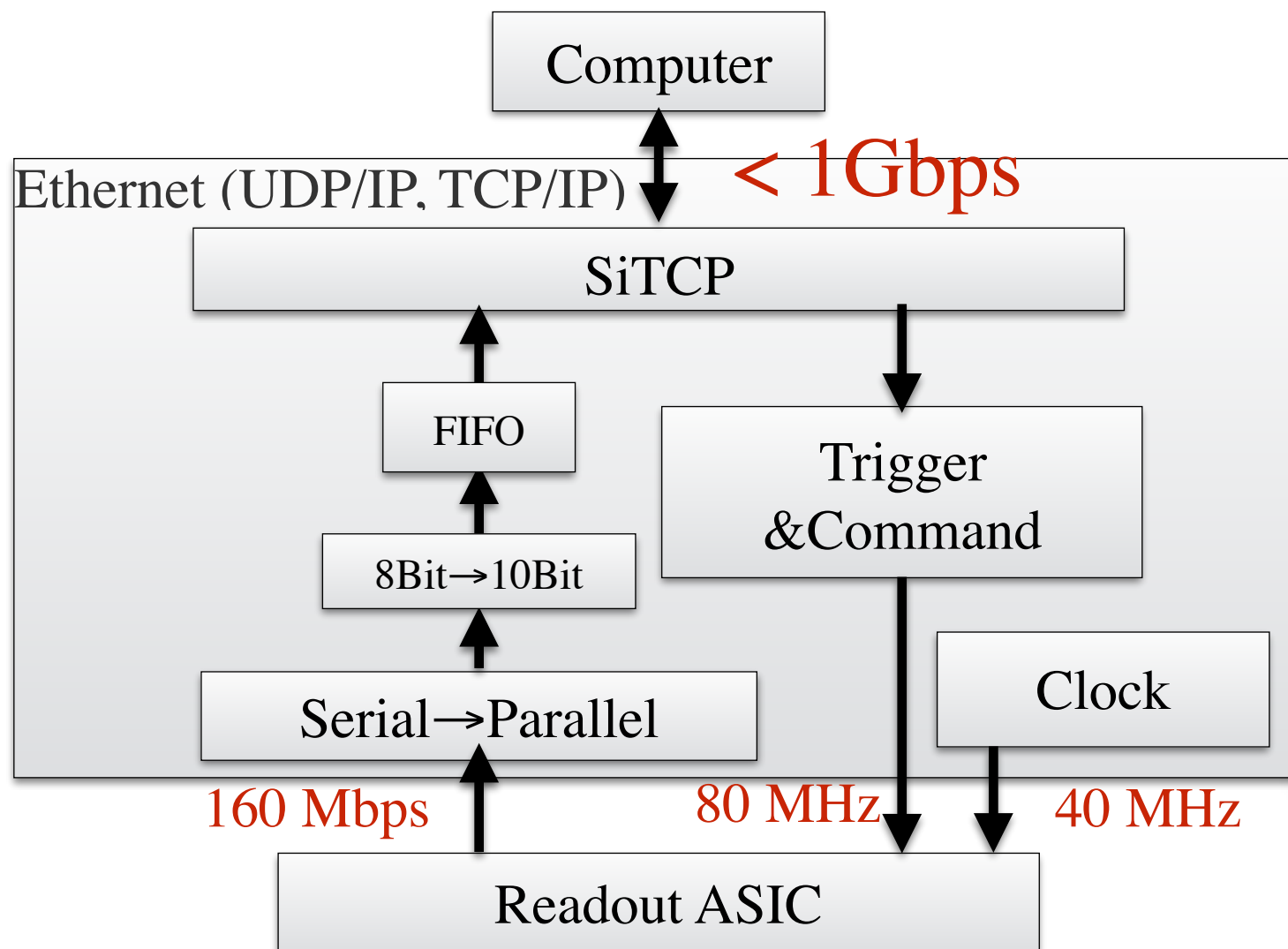
High speed



Xilinx KC705 Evaluation Board

4. ASIC Readout System - Ethernet

1. FE-I4 Readout system using Ethernet

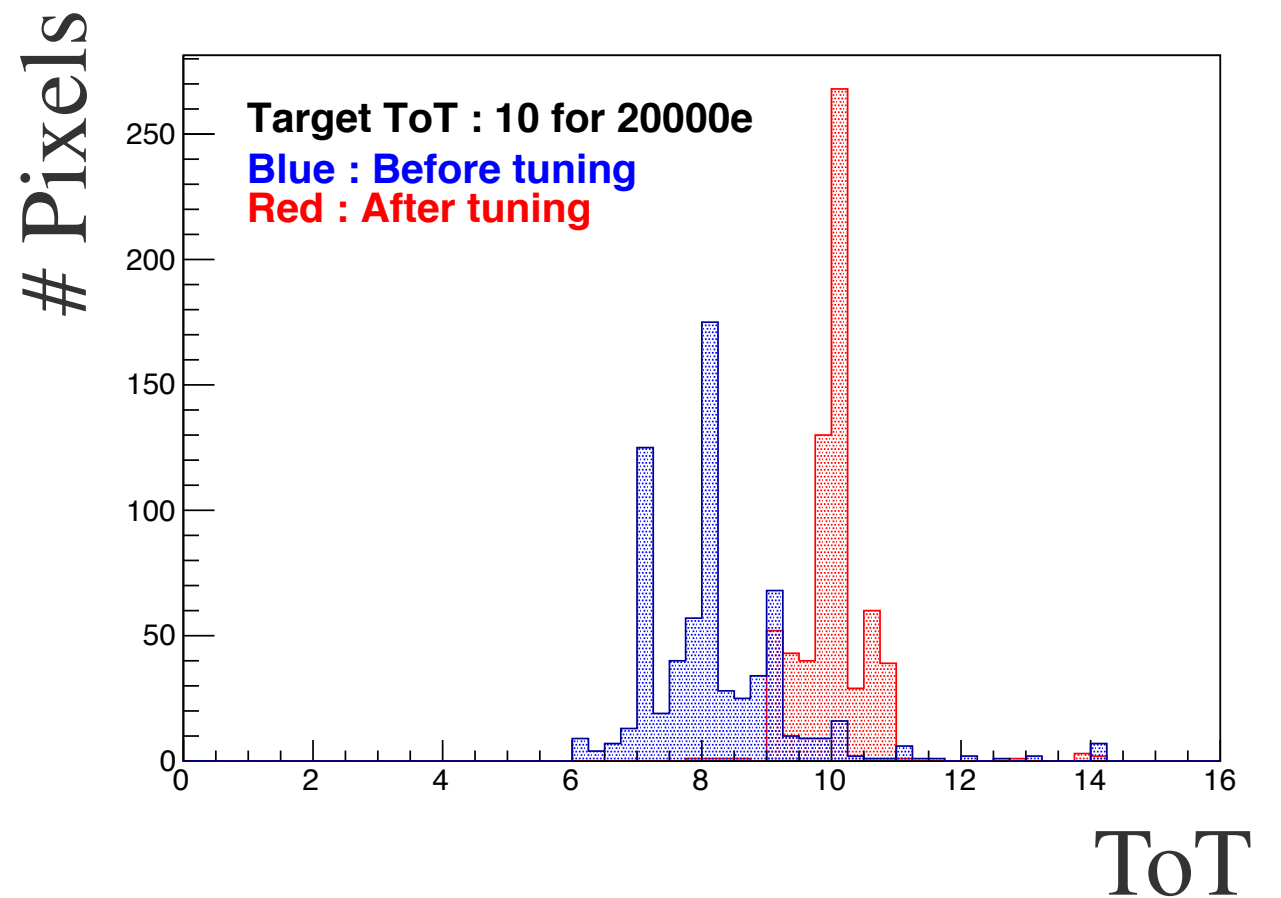
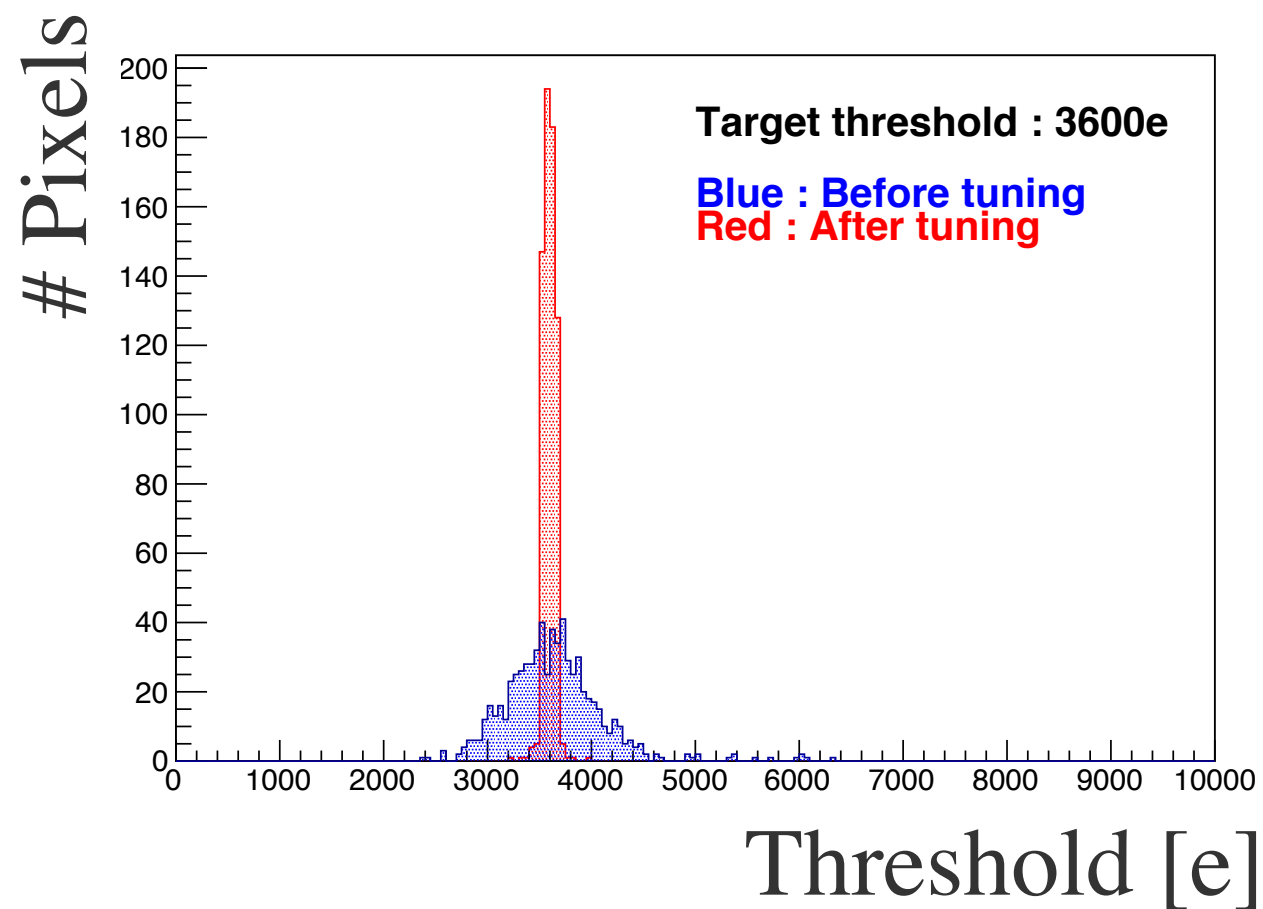


- Implemented in commercially available board !
- Not support 5 Gbps readout, but enough for FE-I4 x4~x6(?)

4. ASIC Readout System - Ethernet

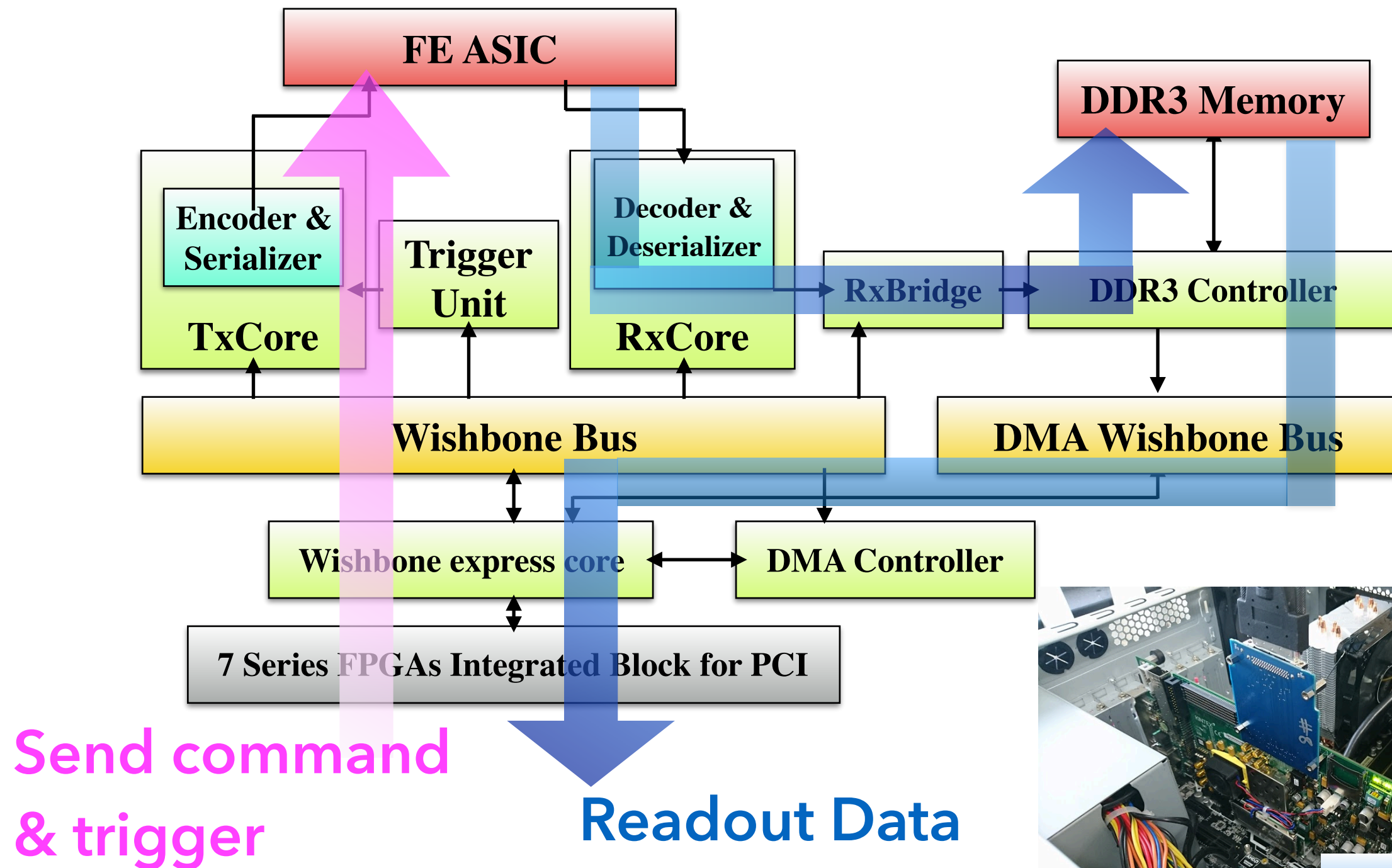
1. FE-I4 Readout system using Ethernet

- Operation Test
 - Tuning of thresholds for Hit
 - Tuning of ToT (like ADC Value) to each pixel



4. ASIC Readout System - PCIe

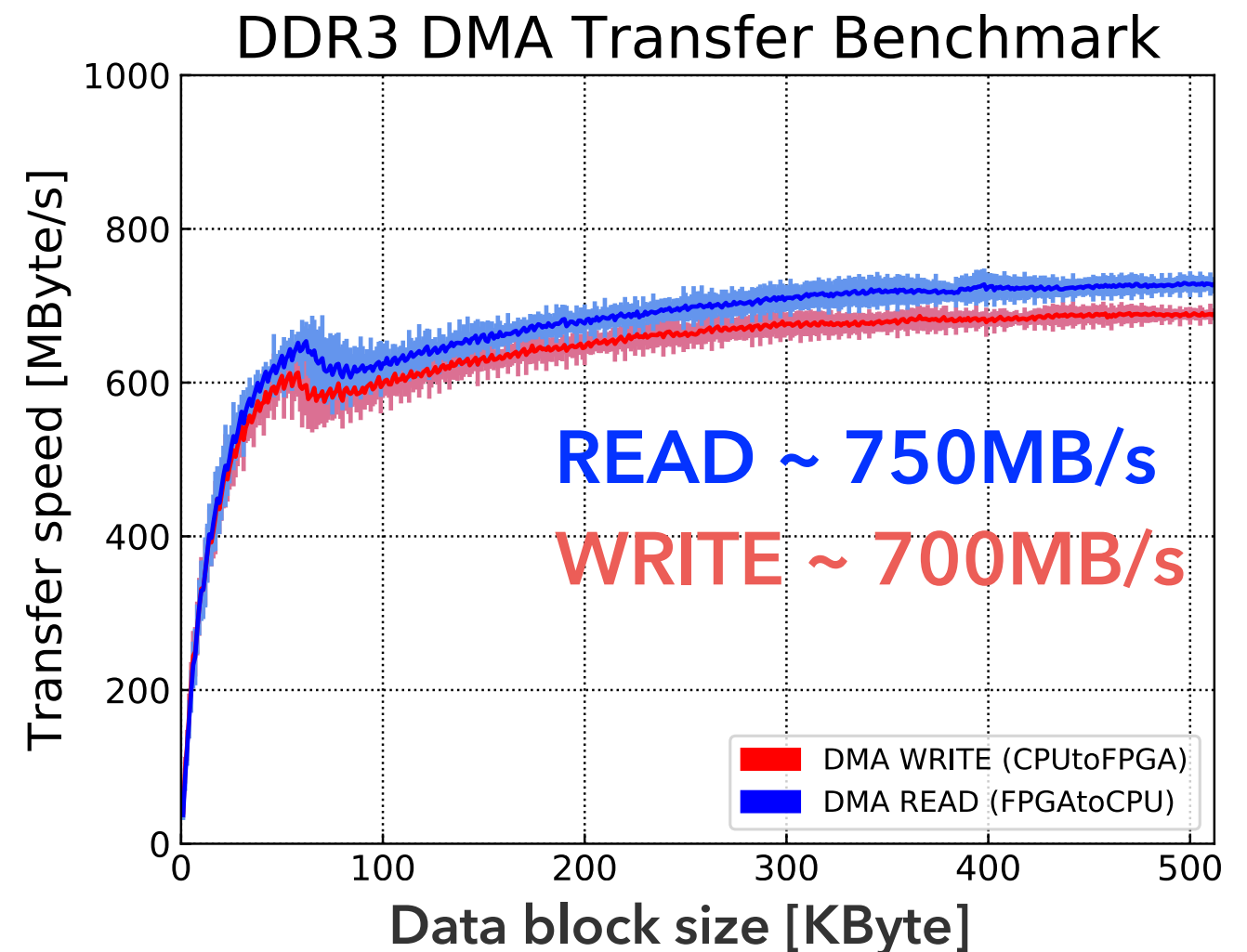
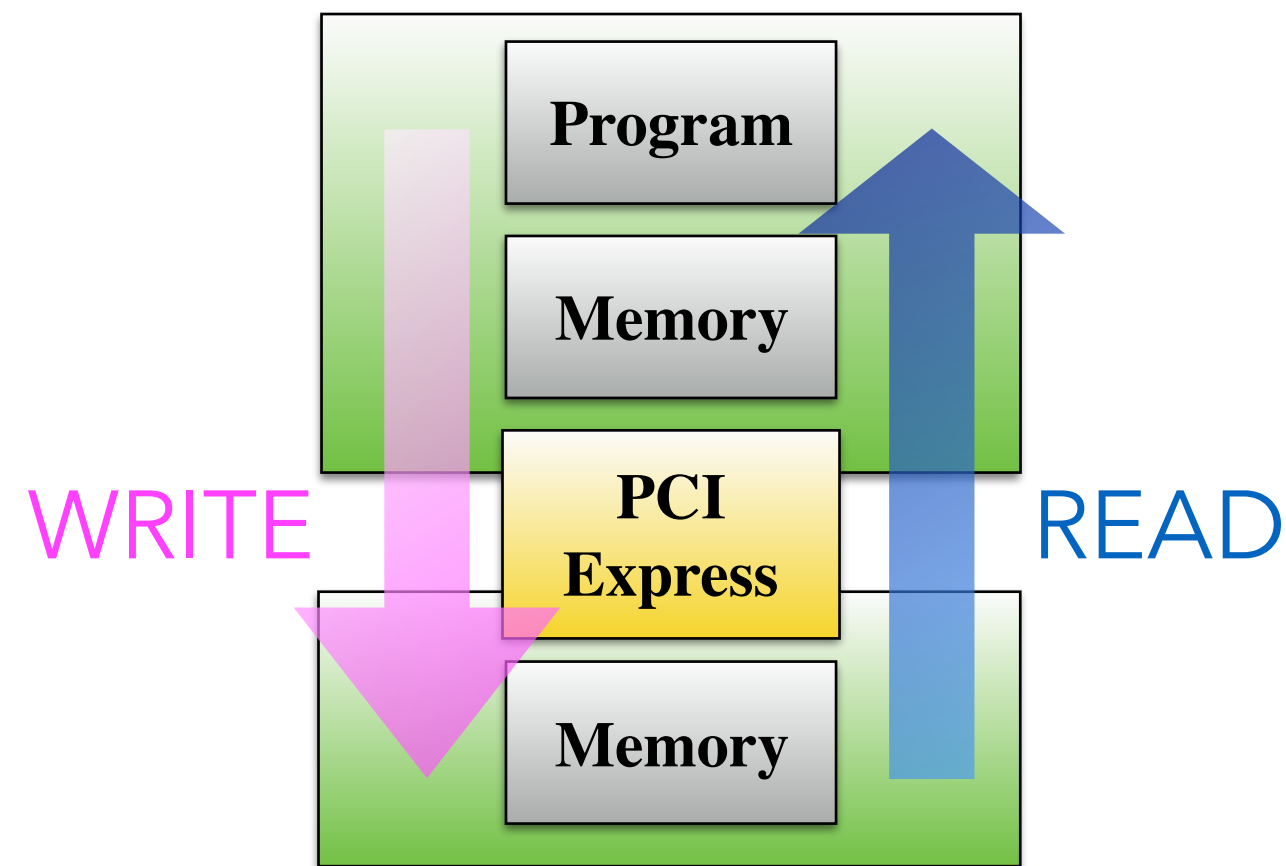
2. FE-I4 Readout system using PCI Express



4. ASIC Readout System - PCIe

2. FE-I4 Readout system using PCI Express

- Direct Memory Access
- PCI Express



5. Summary

- FE-I4 Readout system on KC705 was developed !
- High speed DAQ system
 - Transfer speed performance between FPGA and PC was achieved ! ~750MB/s (READ)
- Future
 - Complete DAQ system
 - + Understanding data transfer performance
 - + Adapt to RD53A

Additional Slides

Development components

Pixel Assembly
Group

Signal
transmission test

Evaluation FPGA Board

FPGA Firmware
DAQ Software

Characteristic test

DAQ Group

Frontend ASIC

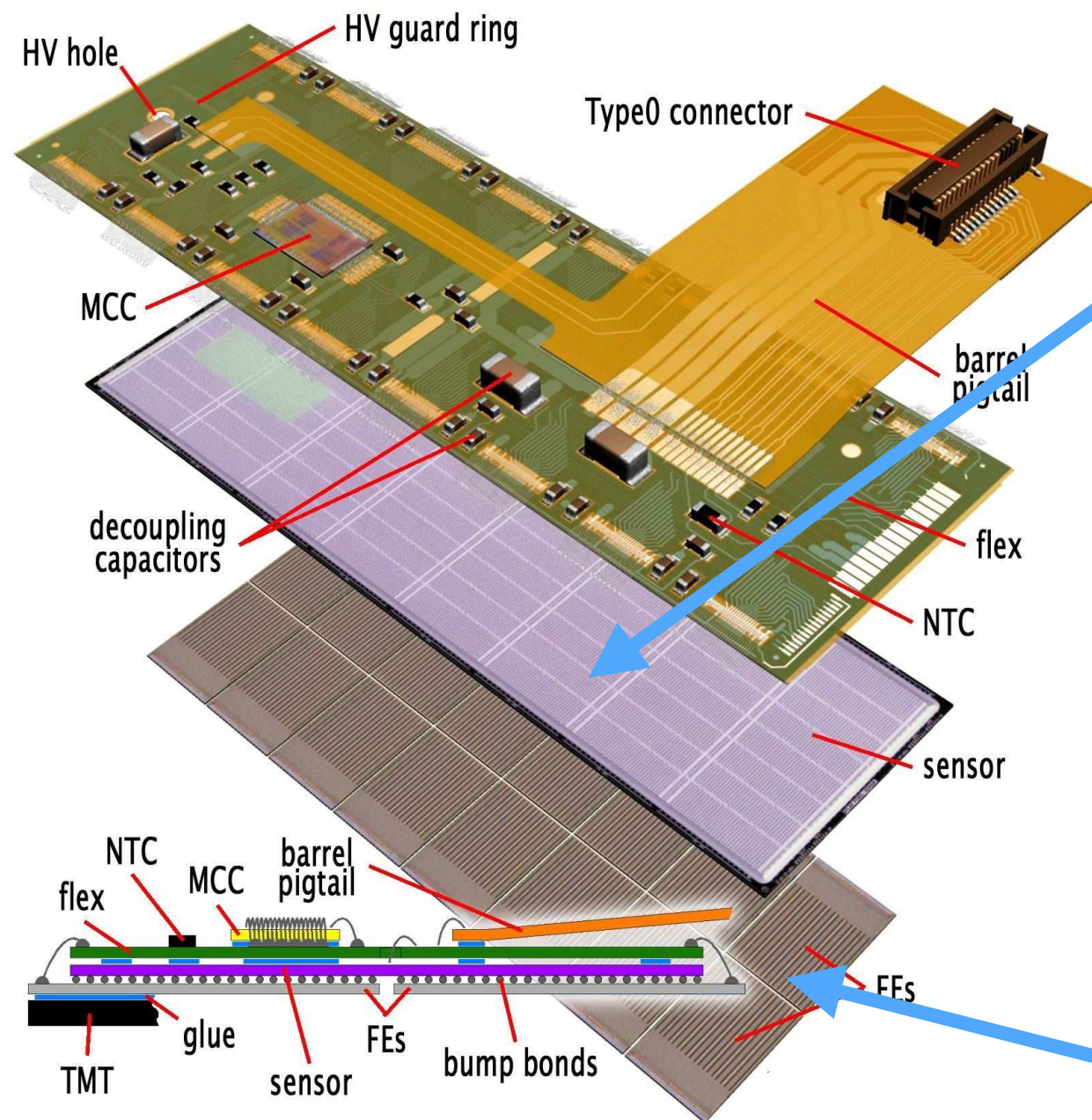
Zynq DAQ System

GitHub

CentOS

2.HL-LHC ATLAS Pixel detector

Pixel detector in ATLAS



Semiconductor Sensor

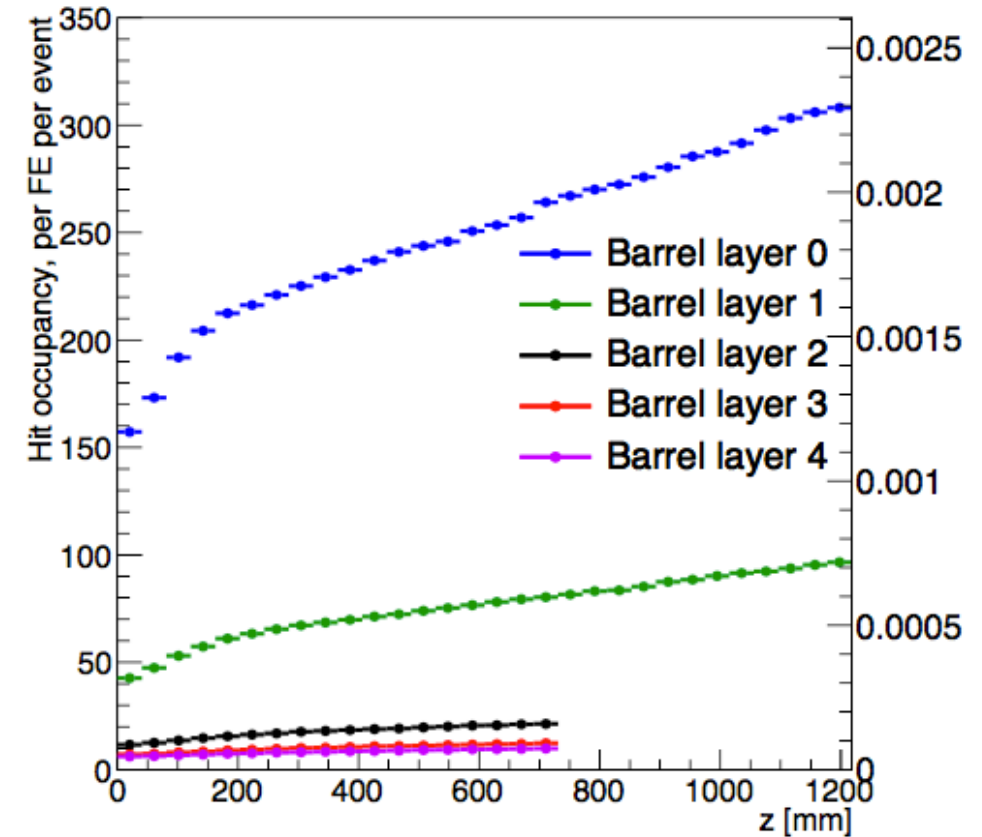
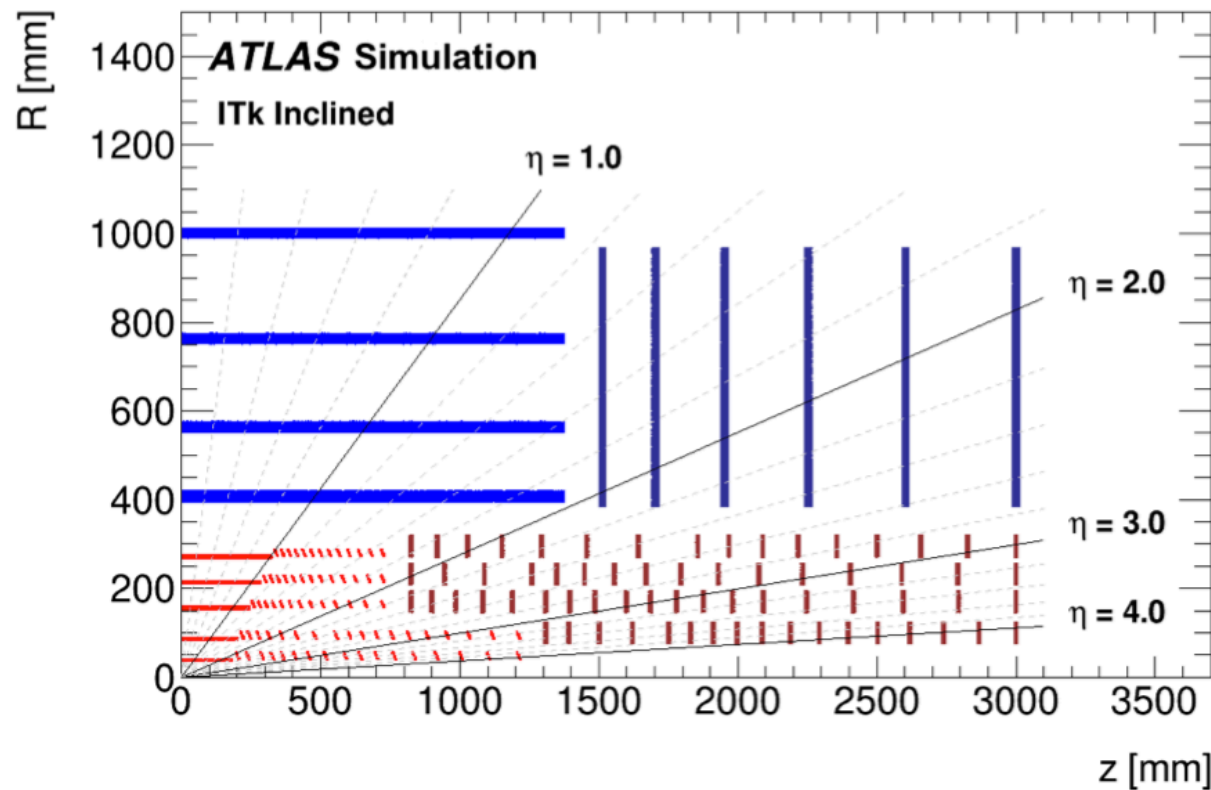
Detect charged particles

ASIC

(Application specific integrated circuit

Digitization of signal
& some functions

Hit rate & Data rate



Detector layer	Number of modules per stave/ring	Module type	Number of links per layer	Data rate per FE [Gb/s]	Data rate per link [Gb/s]
barrel 0	60	dual	1920	4.20	4.20
barrel 1	60	quad	1920	1.30	2.60
barrel 2	36	quad	2304	0.56	1.12
barrel 3	36	quad	1584	0.24	0.96
barrel 4	36	quad	1944	0.21	0.84
ring 0	24	quad	816	0.94	1.88
ring 1	36	quad	1368	0.56	2.24
ring 2	48	quad	1536	0.35	1.40
ring 3	60	quad	1920	0.21	0.84

5 Gbps / chip serial output

- Estimation of requirement 5 Gbps/chip
 - Hit occupancy / FE / event : ~200
 - Data frame length per 1 Hit : 26 bit
 - Trigger rate : 1 MHz

$$200 \text{ Hits/event} \times 26 \text{ bit/Hit} \times 1 \text{ MHz} = \boxed{\sim 5 \text{ Gbps}}$$

(~650 MB/s)

Pixel Sensor readout ASIC prototype (RD53A)

	FE-I4	RD53A
Cell Size	50x250 μm^2	50x50 μm^2 (25x100) μm^2
Pixel Matrix	80x336	400x192
Chip Size	18.2x19.0 mm^2	20.0x2.8 mm^2
Transistor	~80 M	~ 1 G
Input Rate	40 Mbps	160 Mbps
Output Rate	160 Mbps	~5 Gbps
Trigger Rate	200 kHz	1 MHz (L0)
Radiation	300 Mrad	> 500 Mrad
CMOS Process	130 nm	65 nm
Thickness	150 μm	150 μm

Analog pixel schematic diagram

ToT Tuning

Threshold Tuning

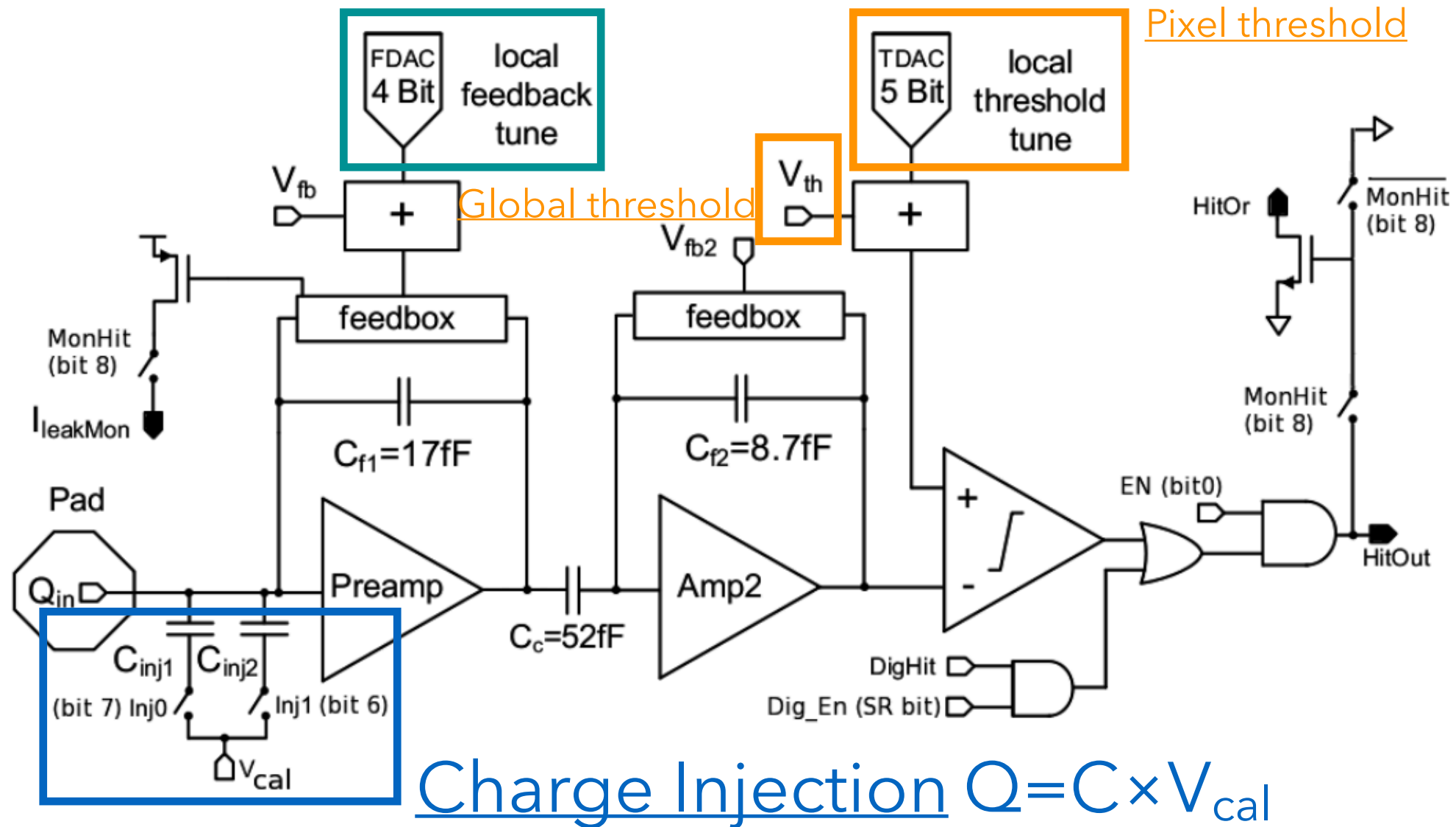


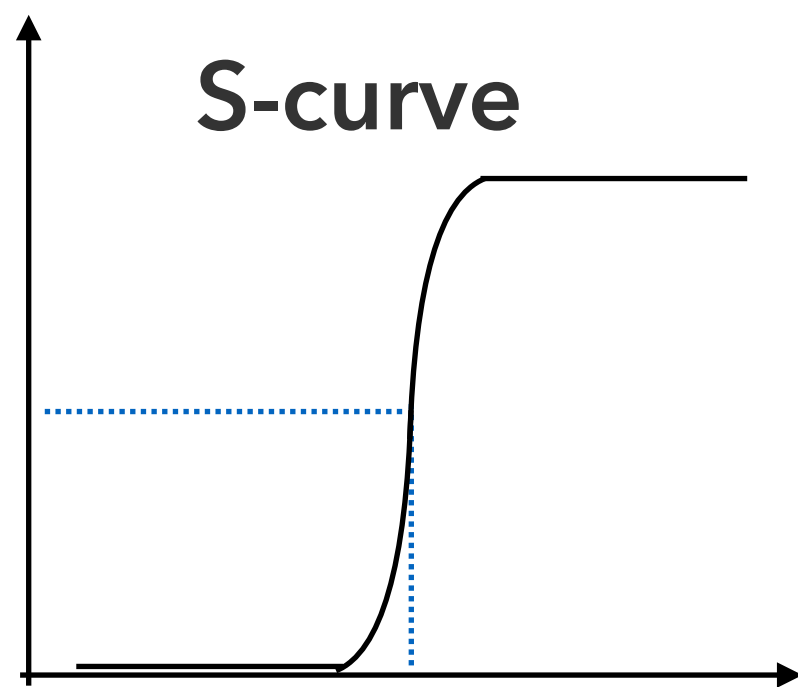
Figure 9: Analog pixel schematic diagram. Output pins are solid, input pins are open.

4. ASIC Readout System

1. FE-I4 Readout system using Ethernet

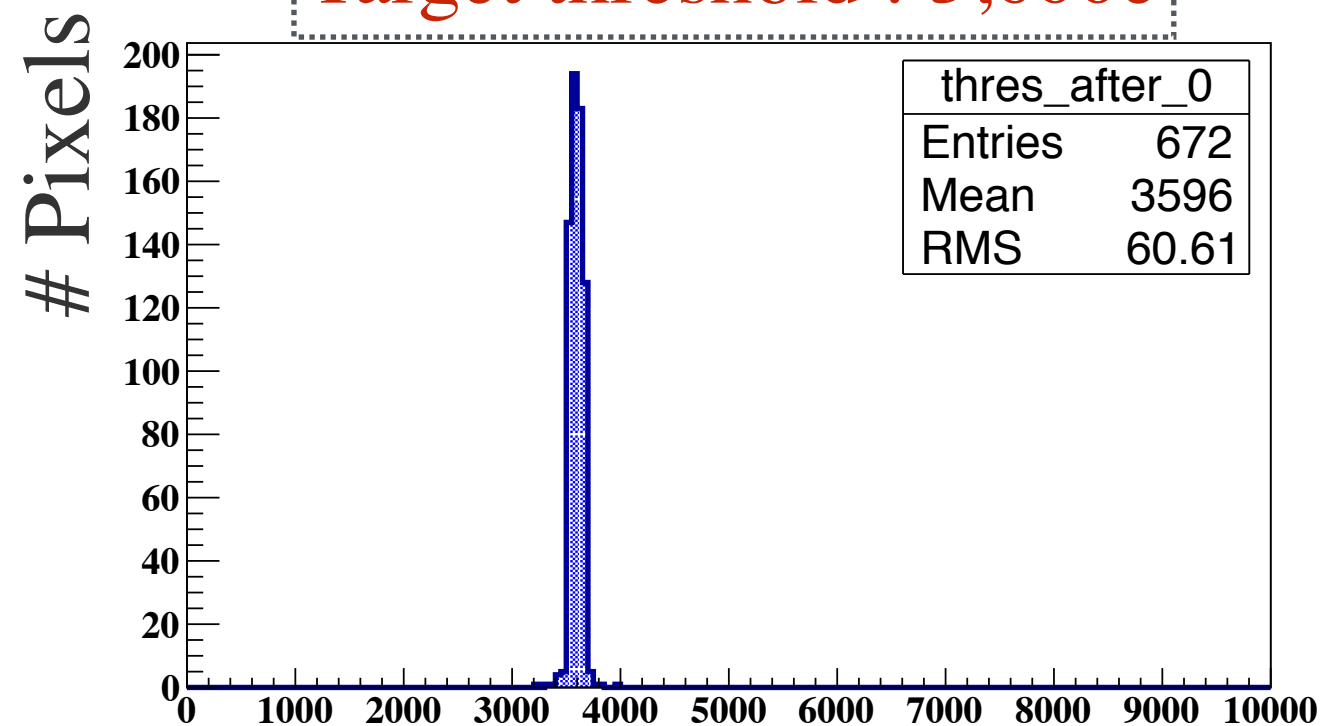
- Operation Test - Threshold Tuning
 - Set Threshold for Hit judgment for each pixel
 - Adjust the feedback current for discriminator to tune target threshold
 - Result was obtained by measurement.

Hit occupancy



PlsrDAC ~ Feedback Current

Target threshold : 3,600e

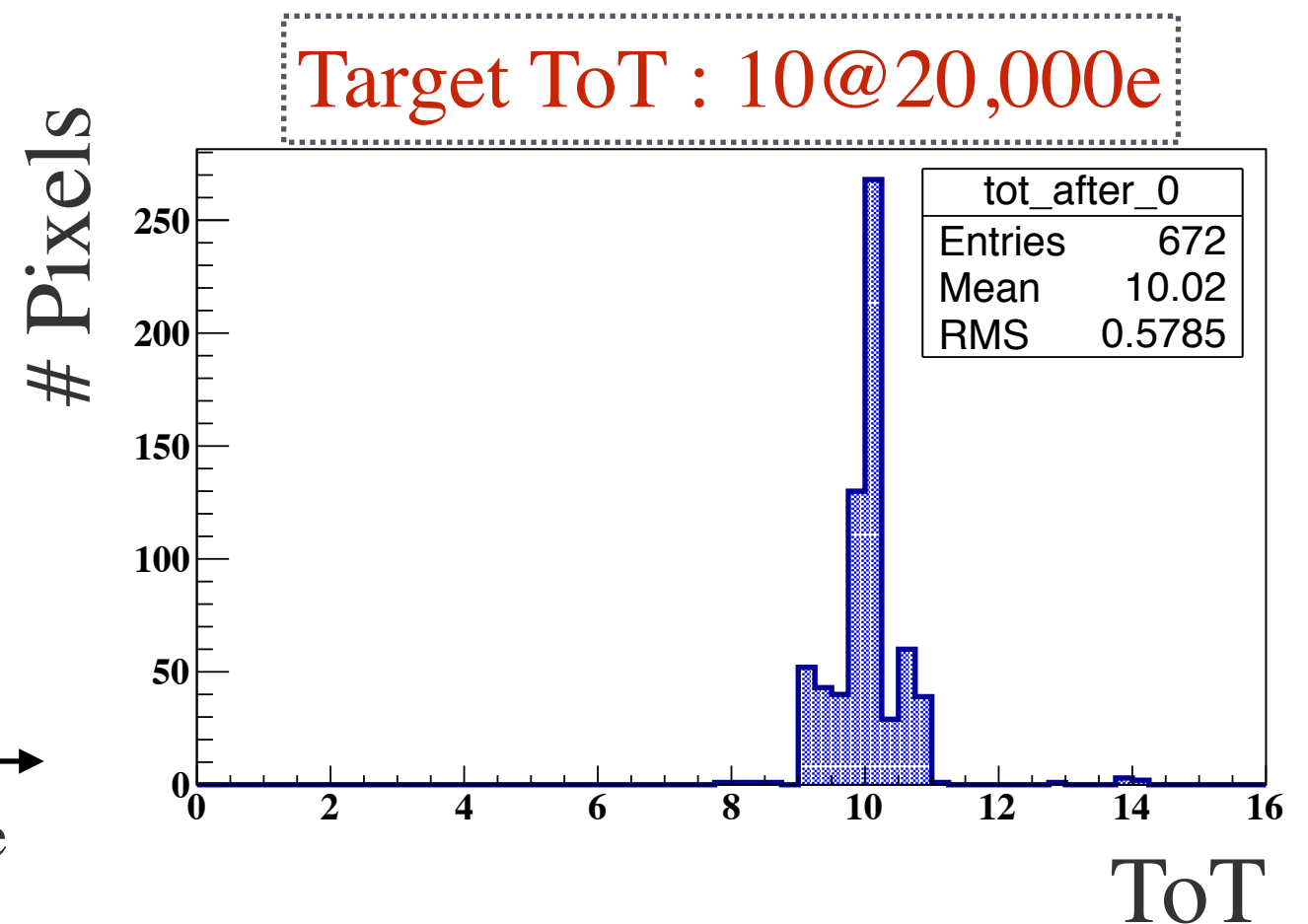
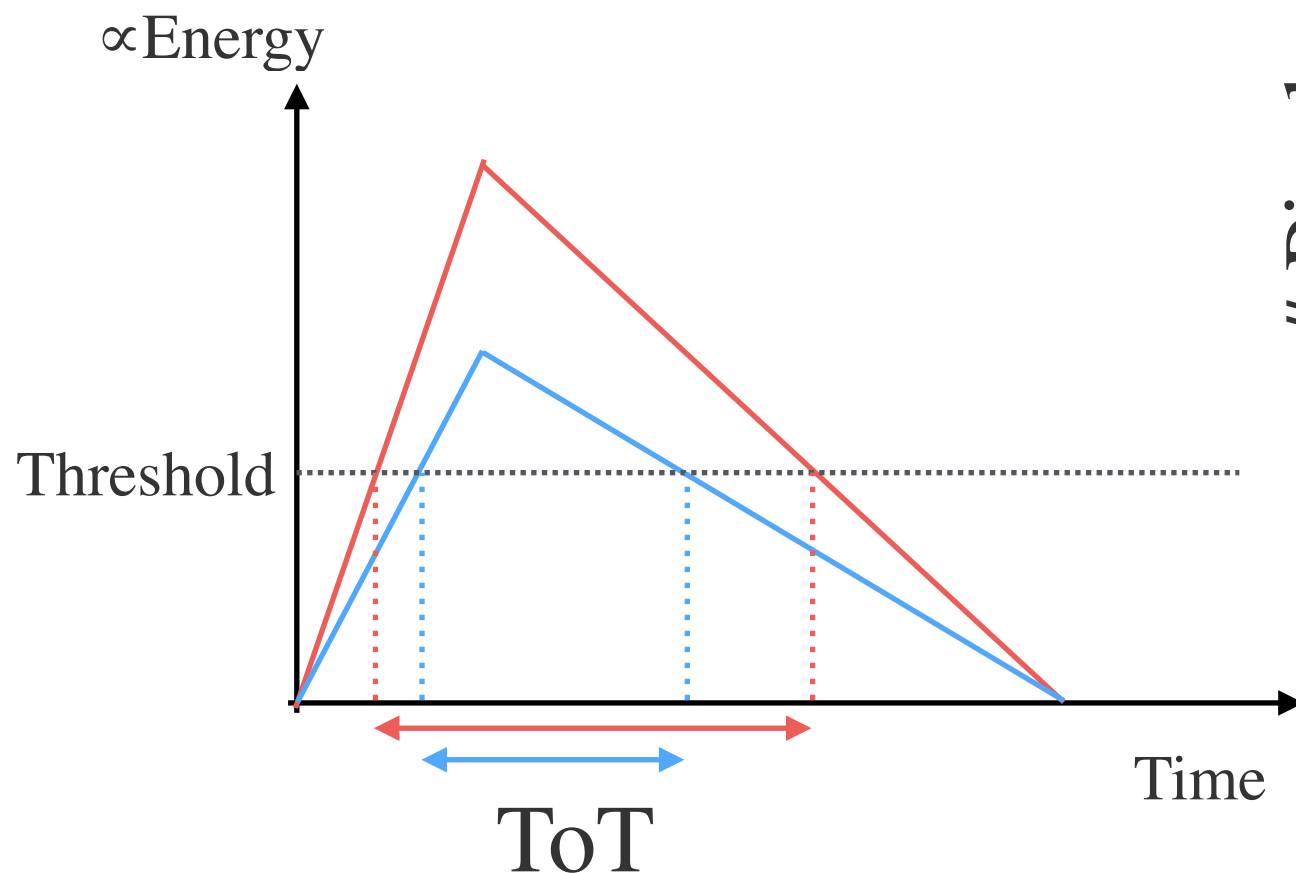


Threshold [e]

4.ASIC Readout System

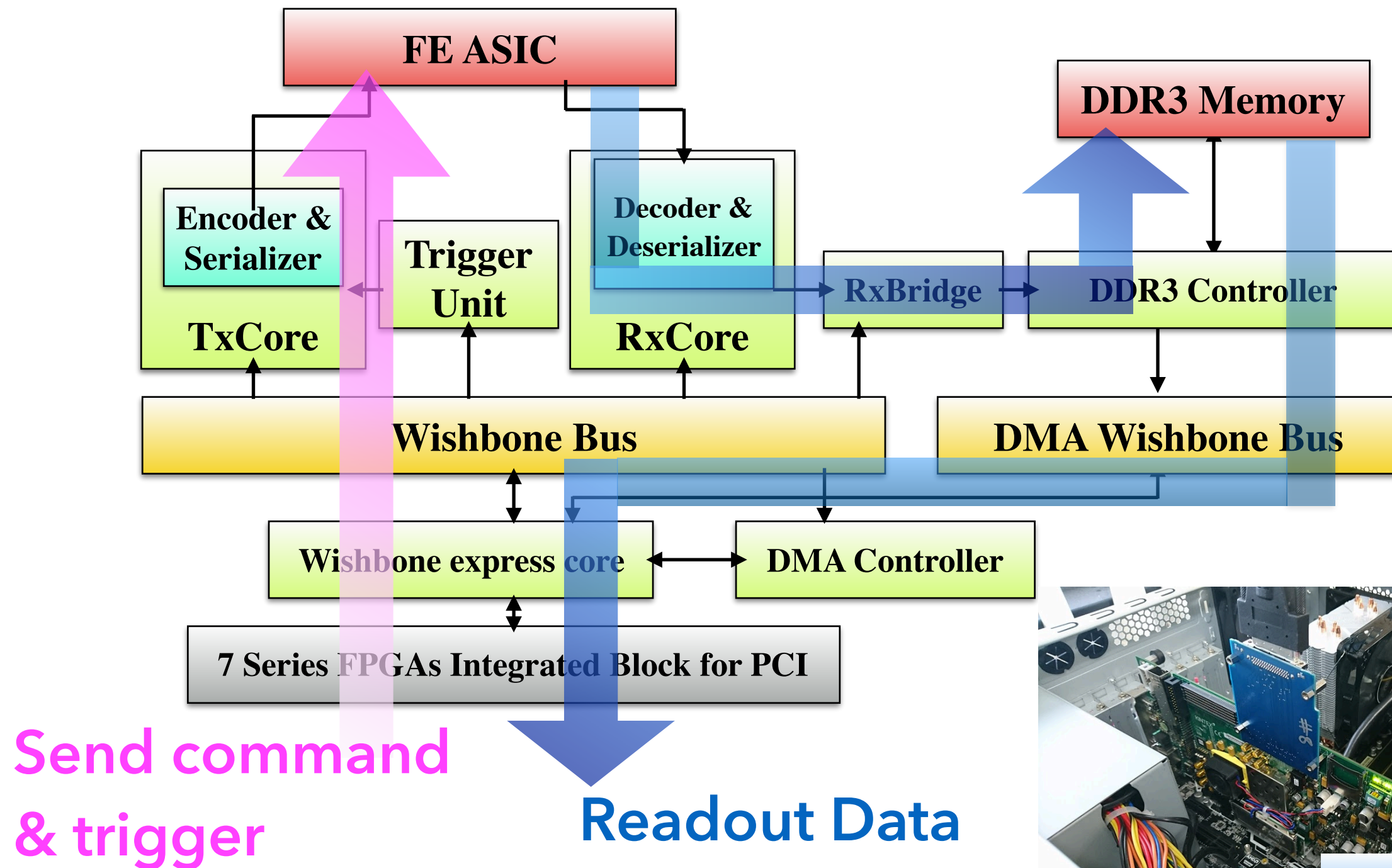
1. FE-I4 Readout system using Ethernet

- Operation Test - ToT(Time over threshold) Tuning
 - ToT is determined with input charge amounts
 - Adjust the feedback current for preamp to tune target ToT.



4.ASIC Readout System - PCIe

2. FE-I4 Readout system using PCI Express



DMA Operation time

- Operation Time of DMA transfer obtained by gettimeofday()

Left : Transfer time + Memory Allocation Time + a

Right : Memory Allocation Time + a

