Development of **SiTCP** Based **Readout** System for **Pixel** Detector **Upgrade** in **ATLAS** Experiment

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Overview

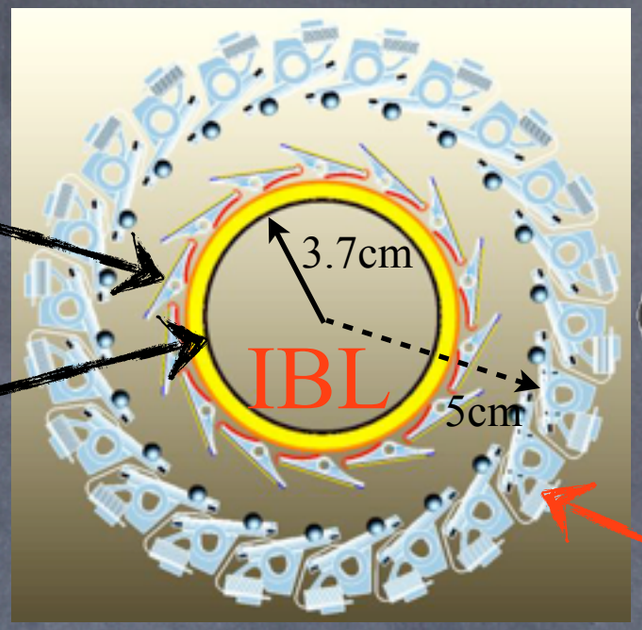
- ATLAS Pixel Detector Upgrade
  - -IBL & S-LHC
  - -New FE chip
  - -New r/o system
- SiTCP Based R/O system
  - -System Interface
  - -What & why SiTCP?
- Module's Setup
- Status & Plan
- Summary

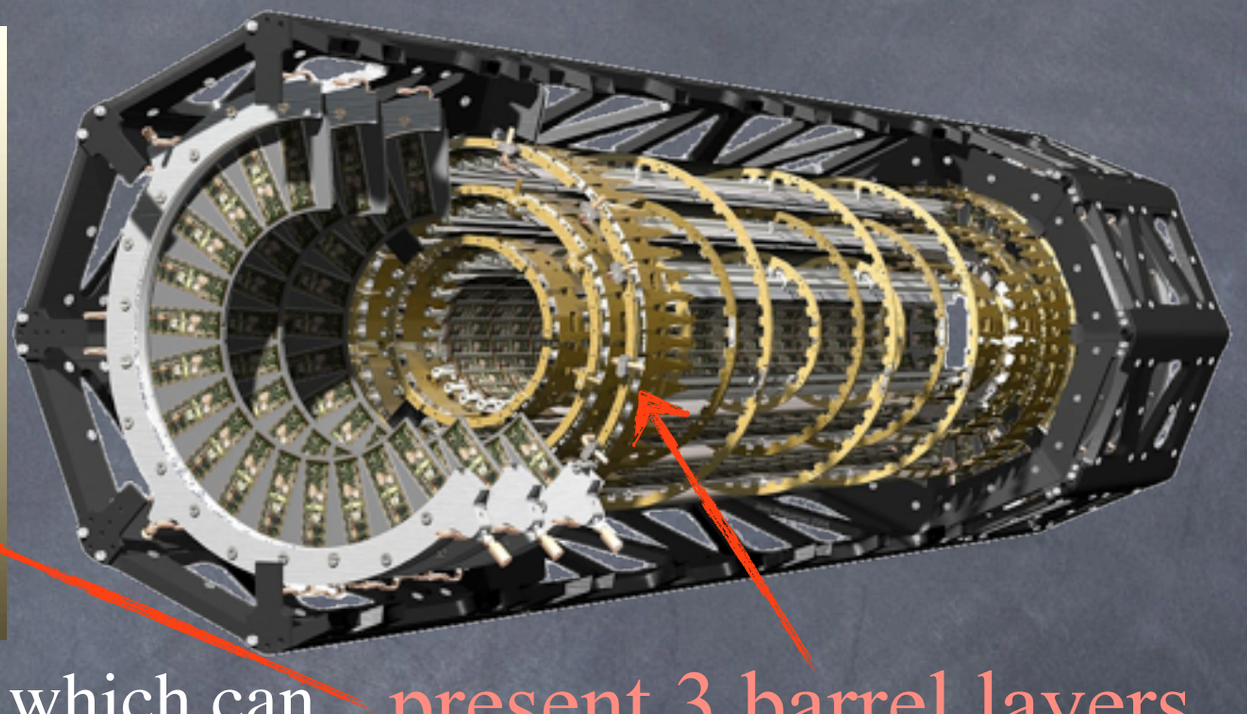
①Intro: ATLAS Pixel Detector Upgrade

IBL = Insertable b-layer

FEi4 mounted on beam pipe

new beam pipe





present 3 barrel layers

Phase 1 (~2015): upgrade to configuration which can eventually deliver **$3x10^{34}$ cm^{-2} s^{-1}.**

Phase 2 (~2019): upgrade to enable SuperLHC luminosity of **10^{35} cm^{-2} s^{-1}.**

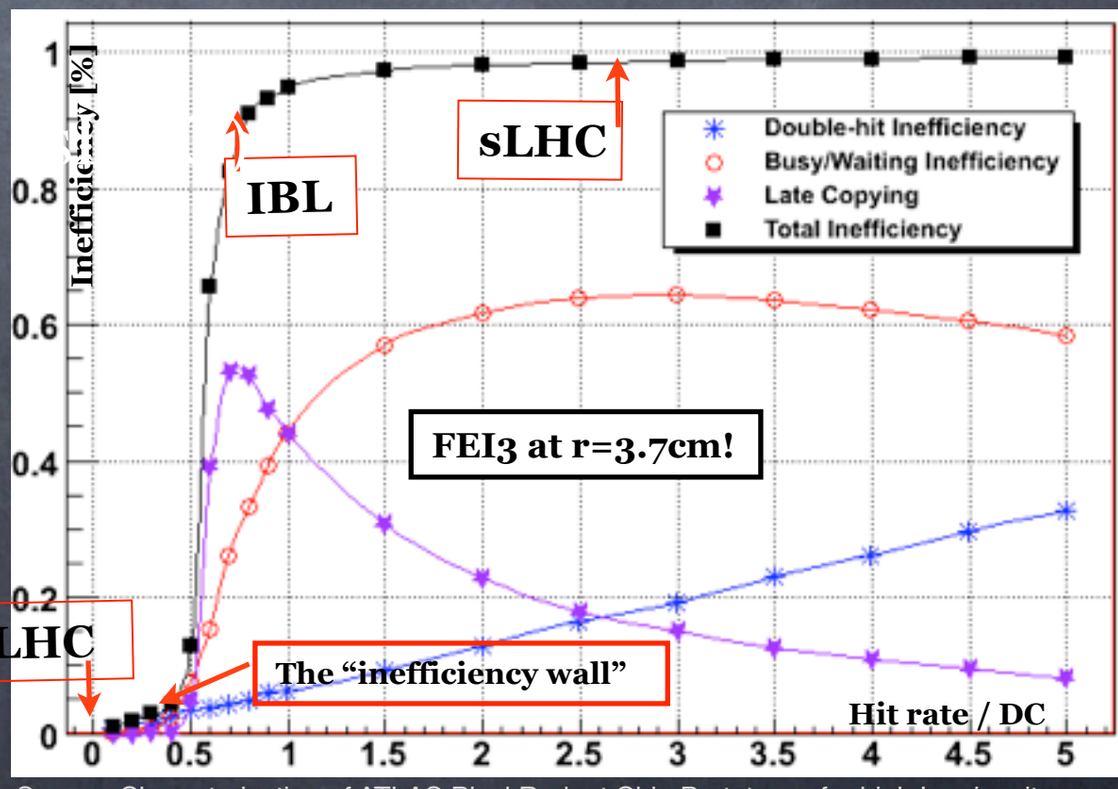
total inefficiency is no longer tolerable

↓

Need for a new FE chip **FEI4**

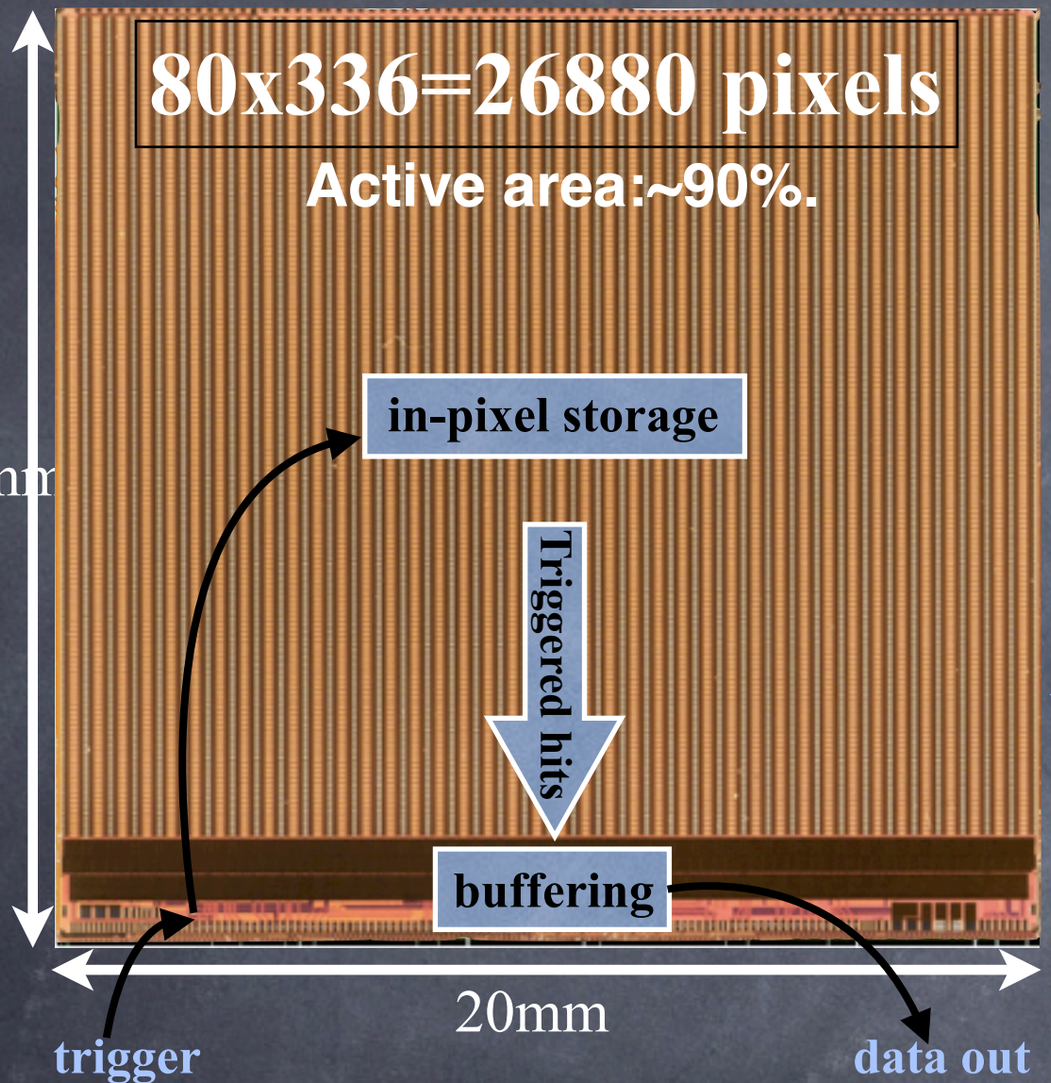
↓

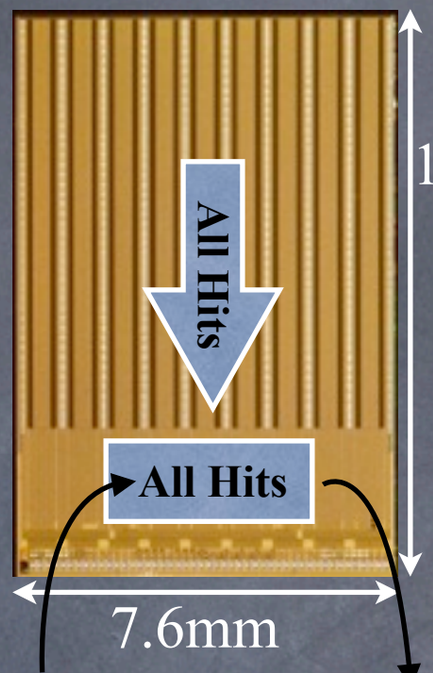
New r/o system is needed!!!



Source: Characterization of ATLAS Pixel Redout Chip Prototypes for high Luminosity Operation of the LHC, Hubertus Junker,, Uni. of Bonn.

Intro: FEi4 Chip





FE-I3: All hits go to periphery (column drain architecture).

FE-I4: local "in-pixel" storage + trigger propagated up the array.

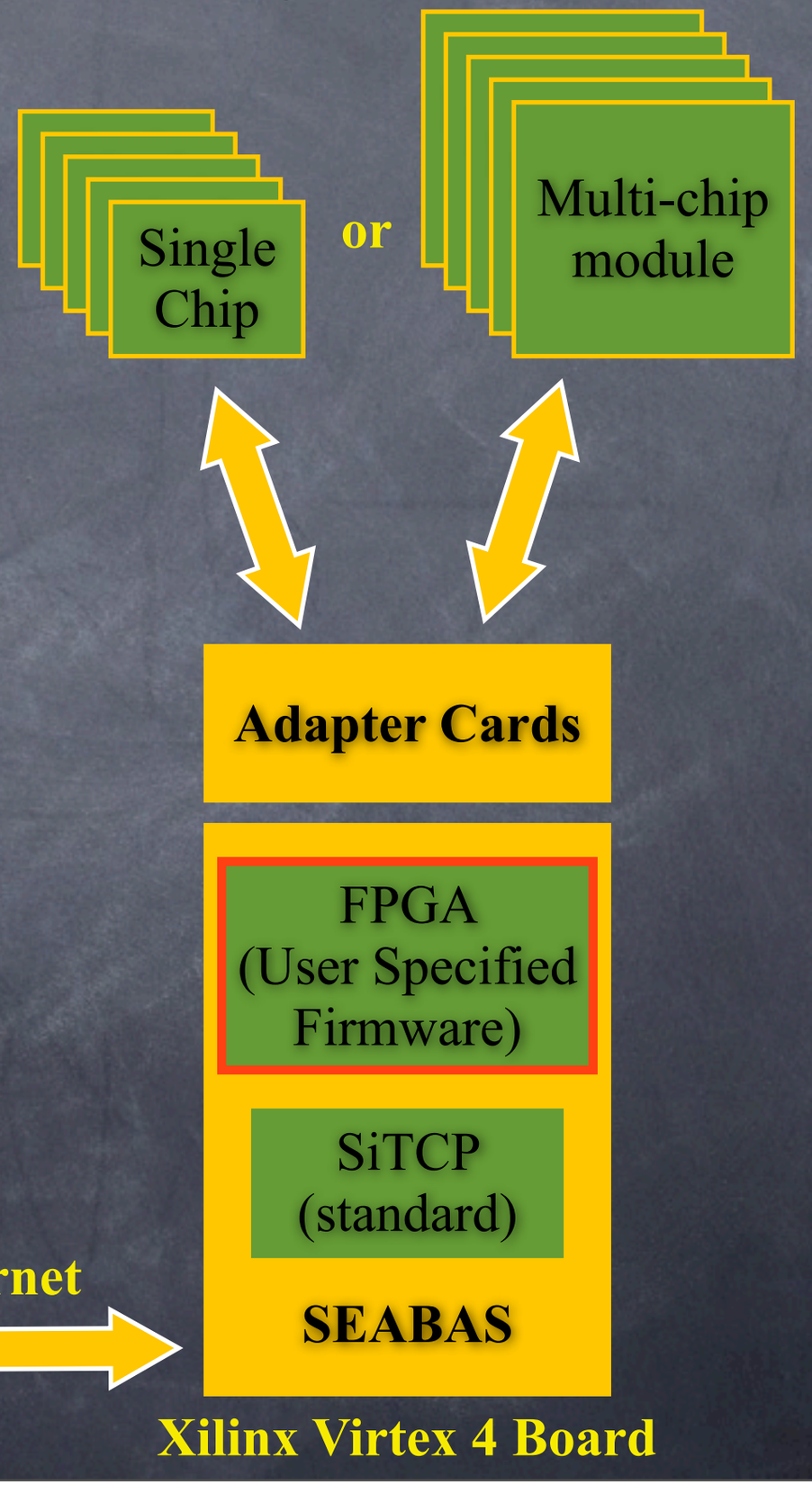
At 3xLHC full lumi, ineff: ~**0.6%**

New features

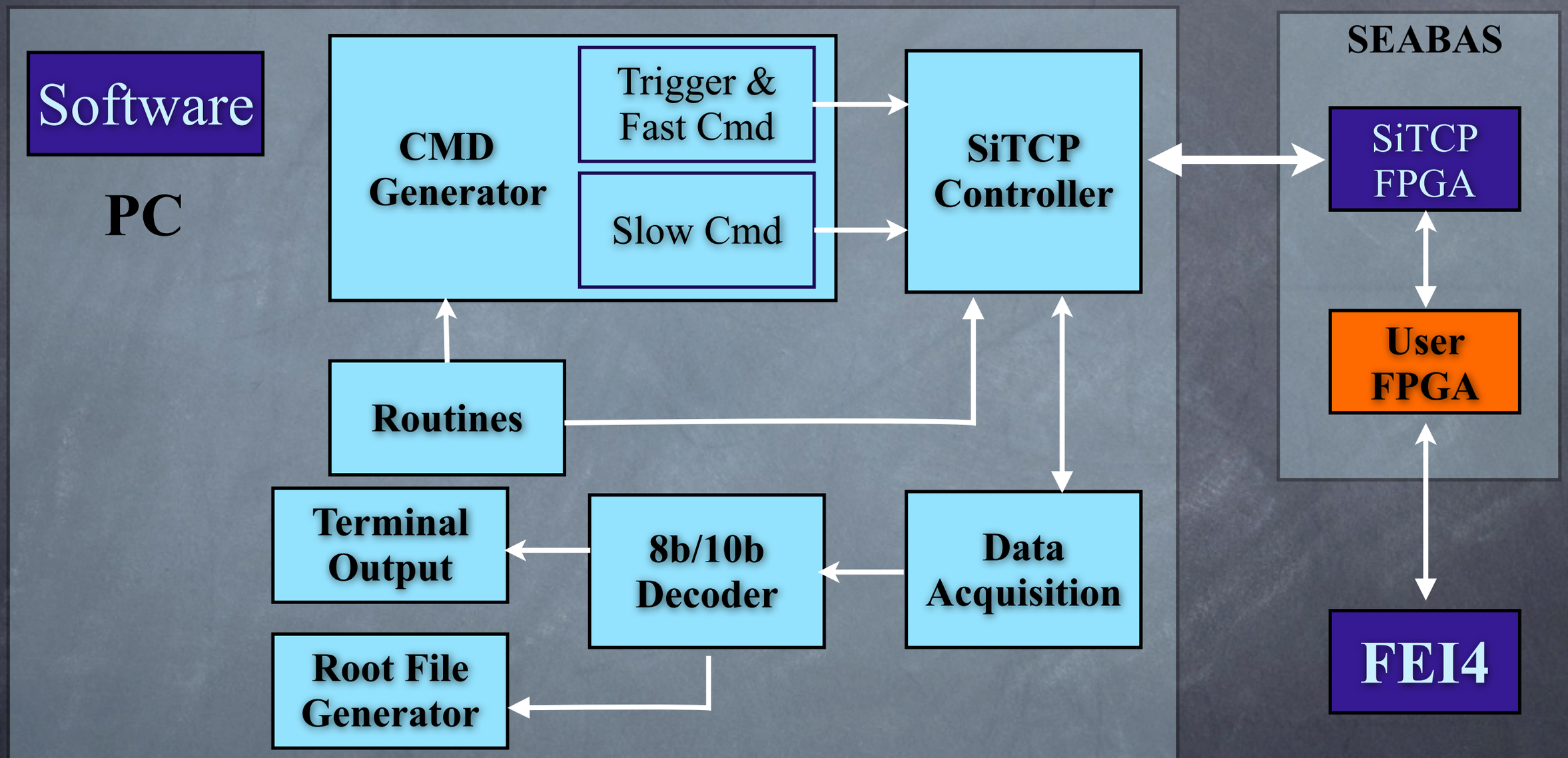
- Biggest chip in HEP to date
- Greater fraction of the footprint devoted to array.
- Lower power comsumption, 10 **μ**W/pixel (un-triggered hits do not move)
- Able to take higher hit rate (store the hits locally in each pixel and distribute the trigger)
- No need for extra module control chip (significant digital logic blocks on array periphery)

② R/O System Interface

- SEABAS (**S**oipix **E**v**A**luation **Bo**A**r**d with **S**itcp)
- One built-in SiTCP FPGA & user FPGA.
- Developed by Tomoshida Uchida (KEK).
- What is SiTCP?
  - a hardware-based TCP processor.
  - designed for devices limited by hardware size (FE devices or detectors).
- Why SiTCP?
  - can be implemented on a single chip due to small circuit size.
  - high speed data transfer (1Gb/s).



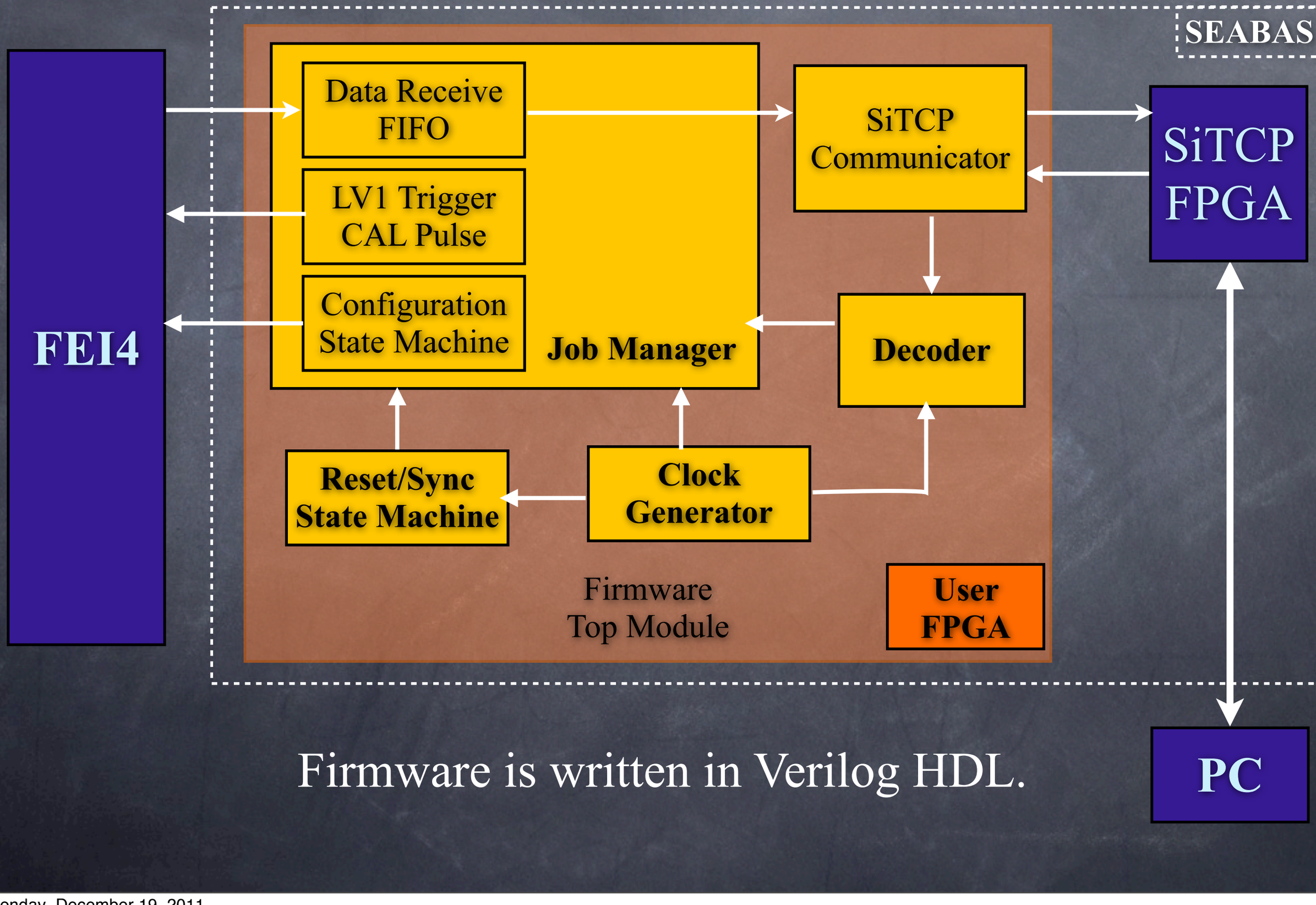
Software Structure



Data stream:

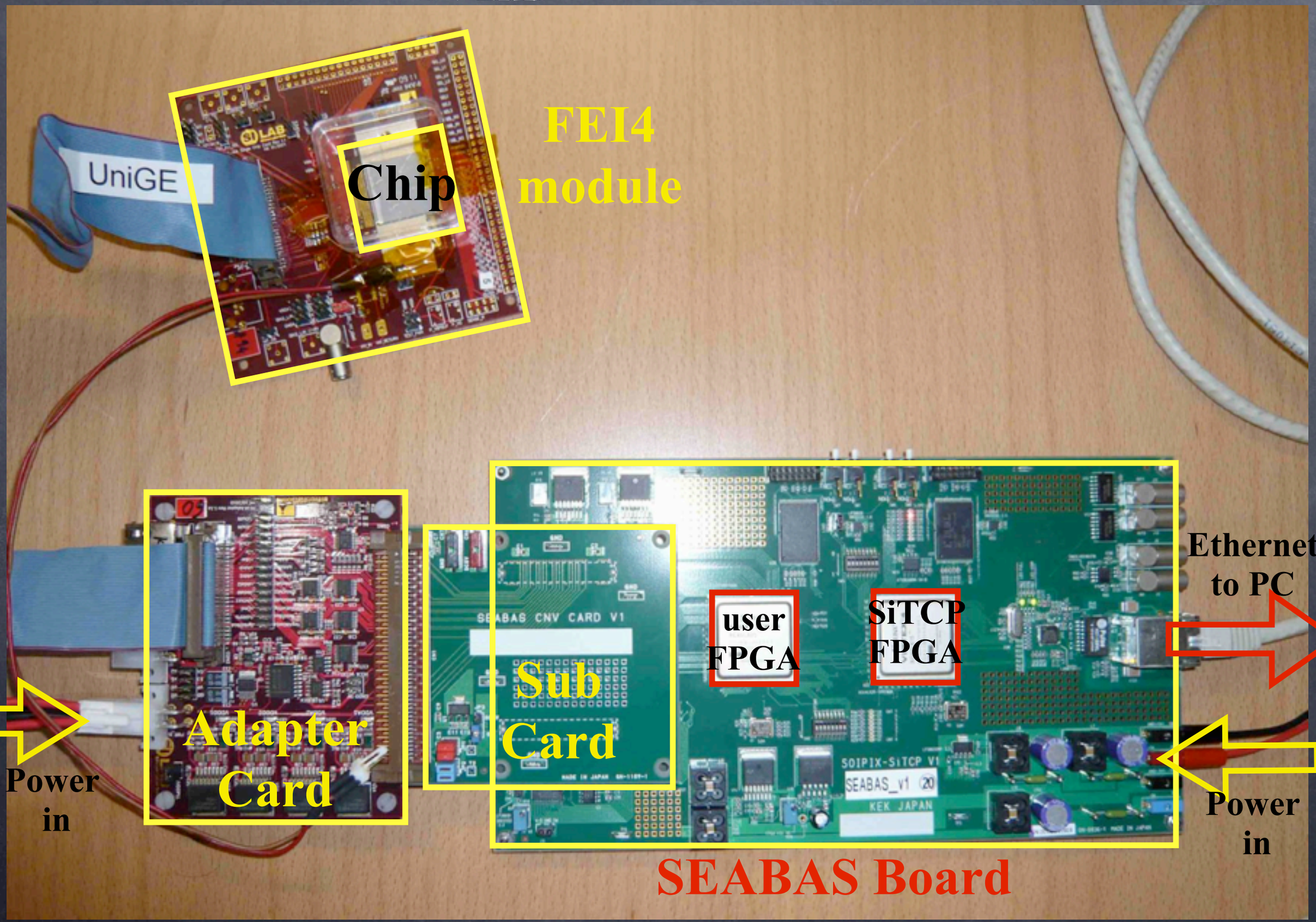
Header 11101...	Data Record 001011101...	Trailer 1000000...

Firmware Structure



Firmware is written in Verilog HDL.

③ Module's Setup



④ Status & Plan

- Phase I: Software and firmware development. **✓ COMPLETED**

  * Special thanks to Yosuke Takubo-san (KEK).

- Phase II: FEi4 chip configuration and debuging. **IN PROGRESS**

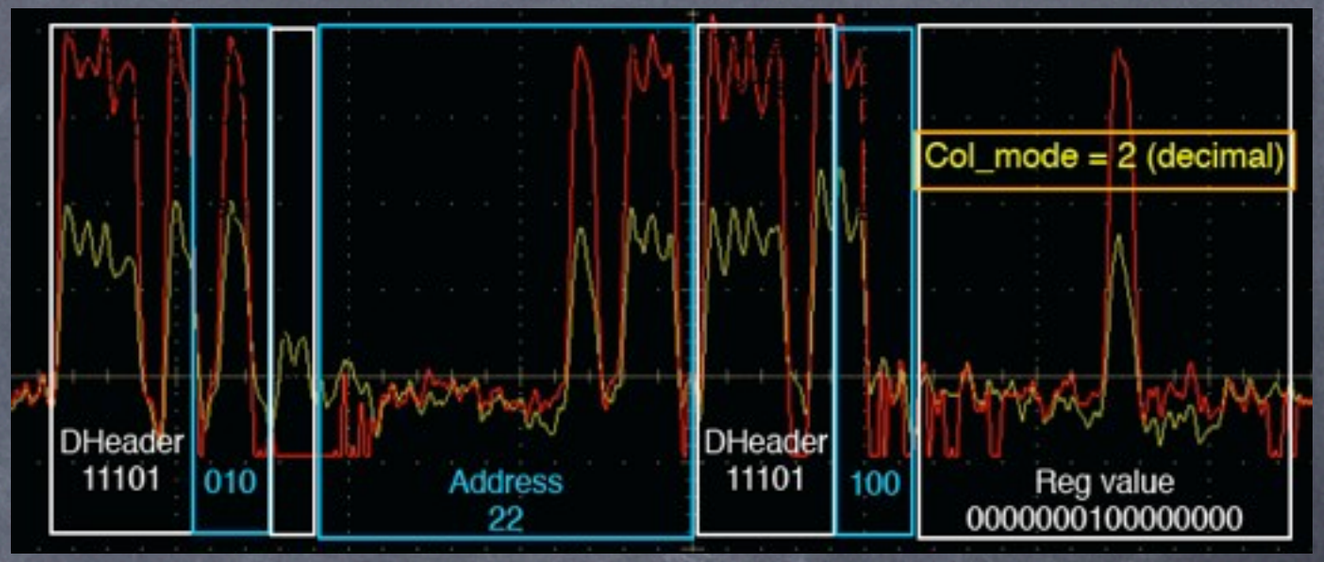
  - Read/write global reg. ✓

  - Read/write pixel reg. ✓

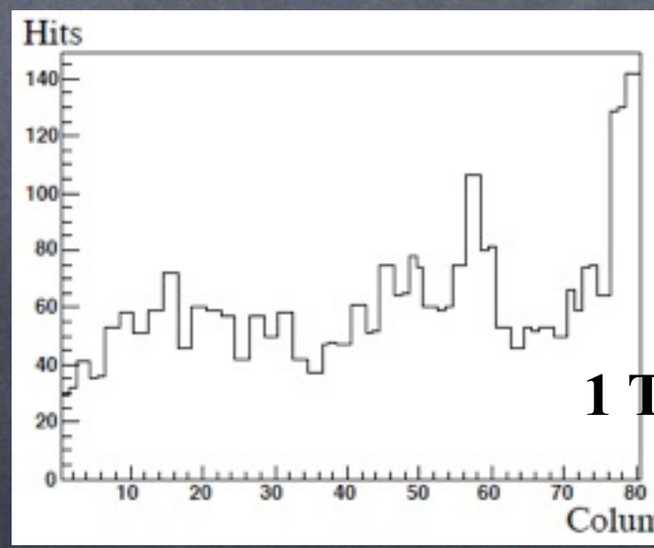
  - A.CAL pulse and L1. ✓

  - Data receiving. ✓

  - 8b/10b data decoding. ✓

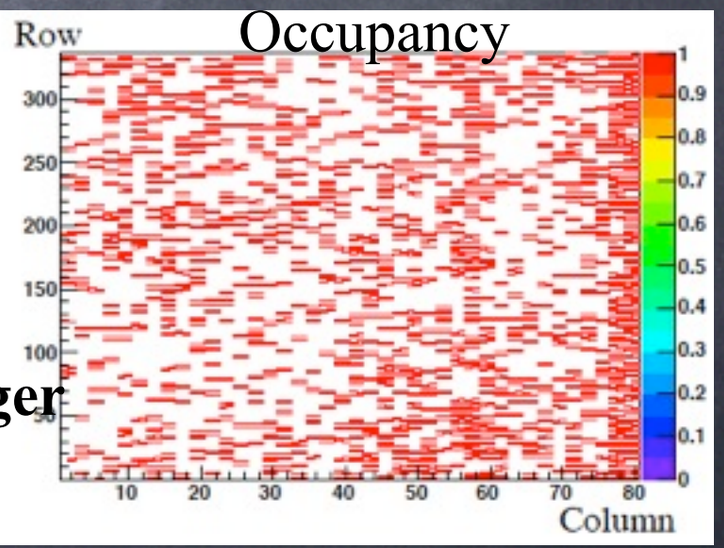


Show Stopper
digital injection



1 Trigger

Occupancy

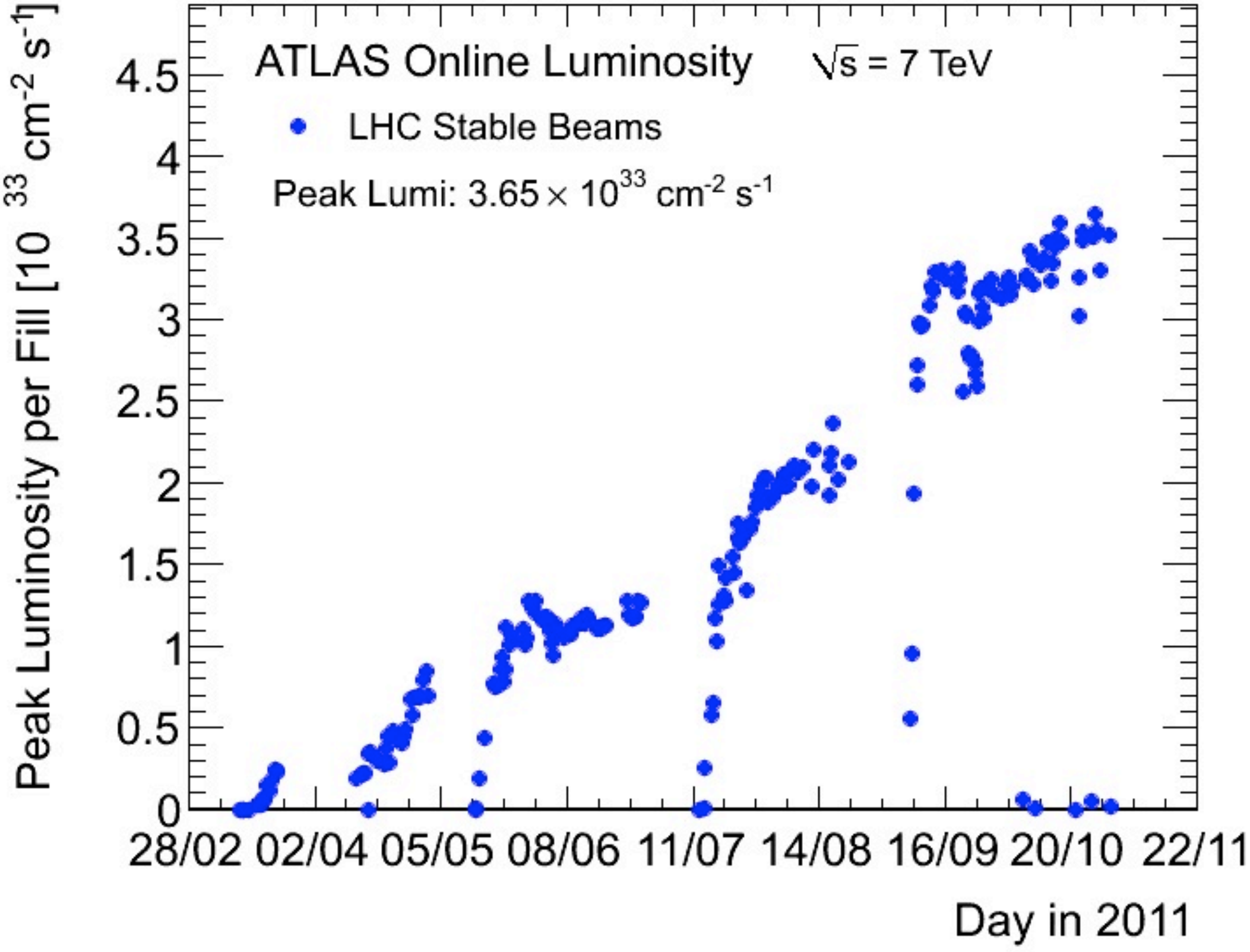


- Phase III: Data acquisition, test and fine tuning. **TO DO** 3rd semester

⑤ Summary

- Skeleton of firmware and software is complete, more functionality will be added.
- Now proceed to operate the chip especially to get the digital injection up and running.
- Aim to get reasonable hit distribution using analog and digital injection test.

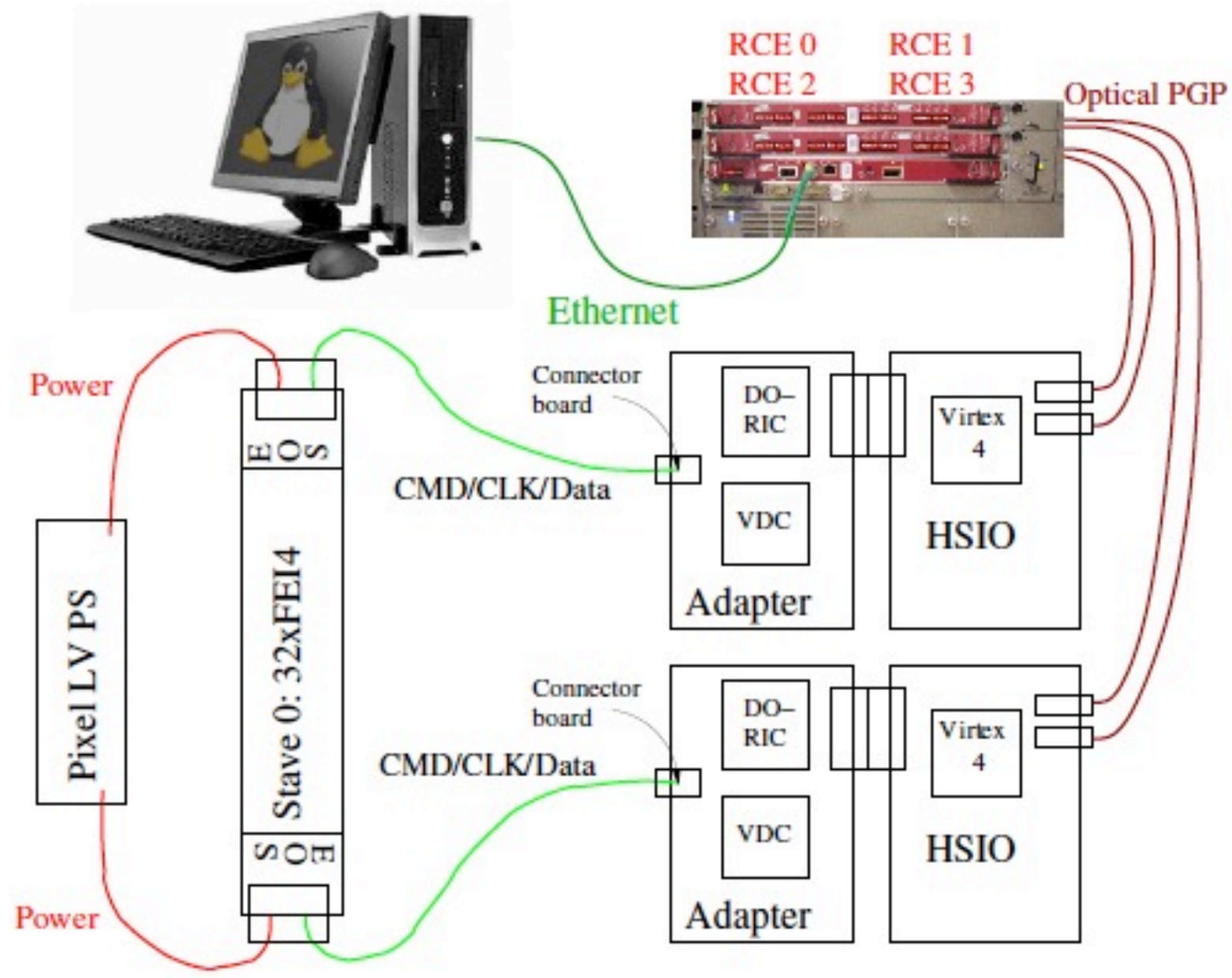
Backup Slides



*only the peak luminosity during stable beam periods is shown.

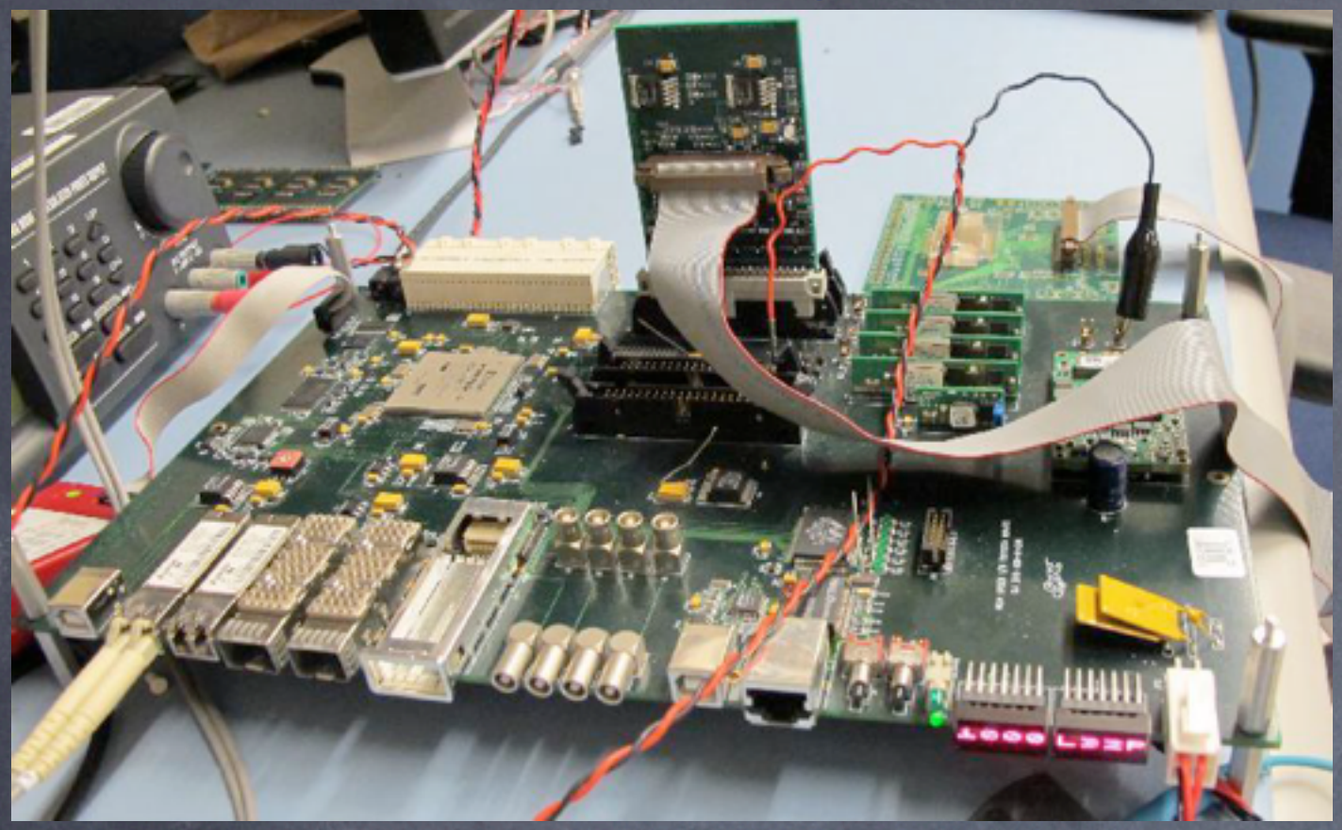
LuminosityPublicResults (21-Nov-2011, JamieBoyd)

Stave -1/0 Hardware Setup

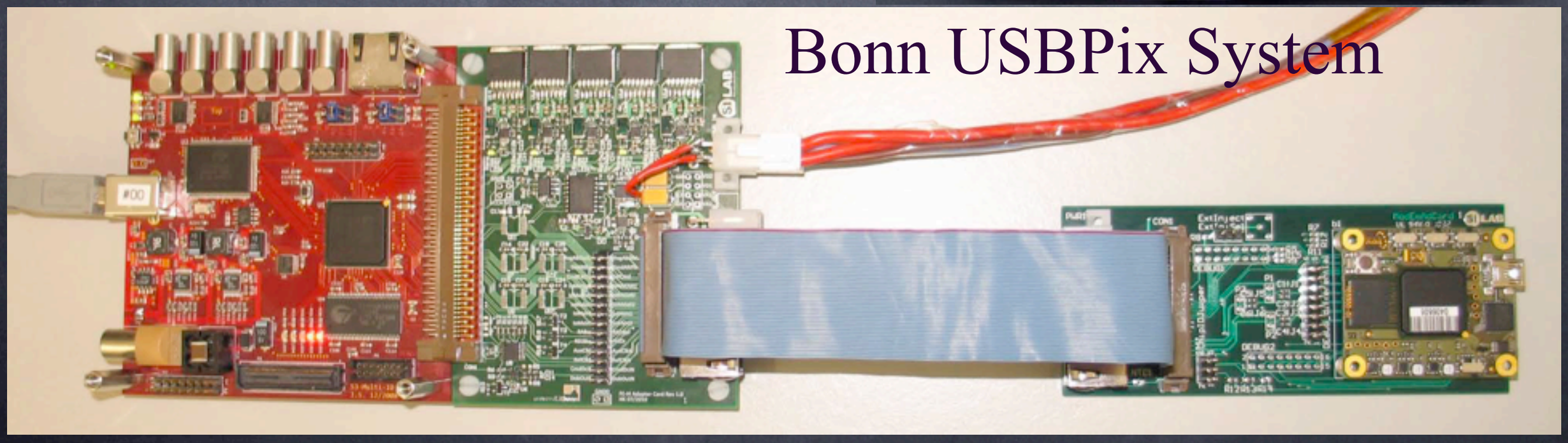


- 4 RCEs / 2 HSIOs.
- 2 adapter boards.

SLAC RCE System



Bonn USBPix System



8b/10b Encoding

- The default output mode of the chip is 8b/10b encoded.
- 8b/10b encoding → - provides data framing and phase alignment.
  → - allows recovery of the 160MHz clock from the data stream in the BOC/ROD in the control room.
- An 8b/10b coder maps the 256 possible “symbols” of an 8-bit word into a specific subset of the 1024 symbols possible for a 10-bit word.
- The selected 10b symbols have some favorable engineering properties:

  - Each 10b word is either perfectly DC-balanced, or has a disparity of +2 or -2. The disparity of a word is defined as the number of 1’s minus the number of 0’s.

  - There is always perfect DC balance over 20 bits. The coder keeps track of DC balance by evaluating a running disparity and compensates for positive or negative disparity with the next word sent.

  - The coder can also generate 12 symbols which have a special meaning, in that they are decoded as commands. These commands are shown in Table 18. These symbols do not have an 8b representation, they only are possible after the 10b encoding.