Development and performance evaluation of the DAQ system used for testing new ATLAS pixel modules for the HL-LHC

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Abstract

The inner tracker system of the ATLAS detector is undergoing upgrades for the High Luminosity-LHC. Due to the increased number of collisions and higher radiation damage, the current pixel detectors in the inner tracker system will be replaced with new ones with better performance. The main part of the improvement can be attributed to the newly developed ASIC (Application Specific Integrated Circuit), which has the ability to transmit data at 1.28 Gbps.

About 10,000 new pixel detectors will be produced in production sites around the world, and Japan plans to produce about 2,000 of them. During this mass production, it is essential to develop a proper testing system for Quality Assurance and Quality Control (QA-QC) of these pixel detectors.

For this testing system, several data adapter cards capable of reading data at high speeds, and power adapter cards capable of powering and monitoring the pixel detectors were developed. The performance of these adapter cards were verified through several independent tests which are reported in this thesis.

From 2020 summer, we have started the production of the first prototypes of the new ATLAS pixel detectors in Japan. Using these pixel detectors, the performance of the overall Data Acquisition (DAQ) system (including the adapter cards) used for testing was verified. Simultaneously, the performance of the first prototype pixel detectors in the world was also verified. Through this, it was confirmed that the developed DAQ system could be used to assure and control the quality of pixel detectors at testing sites around the world.

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List of Abbreviations and Acronyms

AC	Alternating Current.
ALICE	A Large Ion Collider Experiment.
ASIC	Application Specific Integrated Circuit.
ATLAS	A Toroidal LHC Apparatus.
BER	Bit Error Ratio.
BSM	Beyond the Standard Model.
CERN	The European Organization for Nuclear Research.
CLK	Clock.
CMD	Command.
CML	Current Mode Logic.
CMS	Compact Muon Solenoid.
DAQ	Data Acquisition.
DC	Direct Current.
EDA	Electronic Design Automation.
EMI	Electro Magentic Interference.
fb^{-1}	Inverse Femtobarns.
Flex	Flexible PCB.
FMC	FPGA Mezzanine Card.
FPGA	Field Programmable Gate Array.
FR	Flame Retardant.
Gbps	Giga bits per second.

GTX	Gigabit Transceiver.
HL-LHC	High Luminosity LHC.
HV	High Voltage.
IBERT	Integrated Bit Error Ratio Test.
IBL	Insertable B-Layer.
LAr	Liquid Argon (Calorimeter).
LBNL	Lawrence Berkeley National Laboratories.
LDO	Low Drop Out (Regulators).
LHC	Large Hadron Collider.
LHCb	LHC Beauty.
LV	Low Voltage.
Mbps	Mega bits per second.
MMA	Multi Module Adapter.
NTC	Negative Temperature Coefficient.
oz/feet^2	Ounce per square feet.
PCB	Printed Circuit Board.
PCI Express	Peripheral Component Interconnect Express.
PTH	Plated Through Hole.
RX	Receiver.
SCT	Semiconductor Tracker.
SLAC	National Accelerator Laboratory.
SLDO	Shunt-LDO (Regulators).
SMA	Sub-Miniature version A.
SUSY	Super Symmetry.
TRT	Transition Radiation Tracker.
TX	Transmitter.
YARR	Yet Another Rapid Readout.
ZIF	Zero Insertion Force.

Chapter 1

Introduction

1.1 LHC and the ATLAS experiment

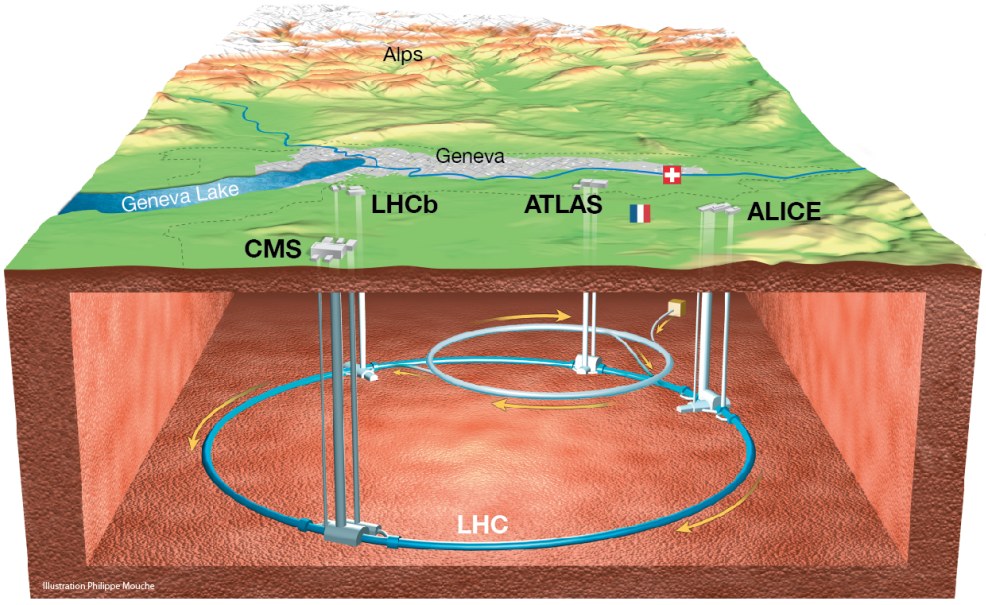


Figure 1.1: An illustration of the Large Hadron Collider, which lies on the Franco-Swiss border, in Switzerland [1].

1.1.1 LHC - The Large Hadron Collider

The large hadron collider (LHC) shown in Figure 1.1 is the largest particle accelerator in the world. It is located in a 27 km long tunnel, 100 m beneath the ground at CERN, the European Organization for Nuclear Research, in Switzerland.

In the LHC, two proton beams are accelerated in opposite directions, and collide at a 13 TeV center of mass energy. These protons beams are bunched, and the bunches (1.2×10^{11} protons per bunch) cross each other every 25 ns.

At the collision points of the proton beams, four LHC experiments are conducted; ATLAS, CMS, LHCb and, ALICE.

1.1.2 The ATLAS experiment

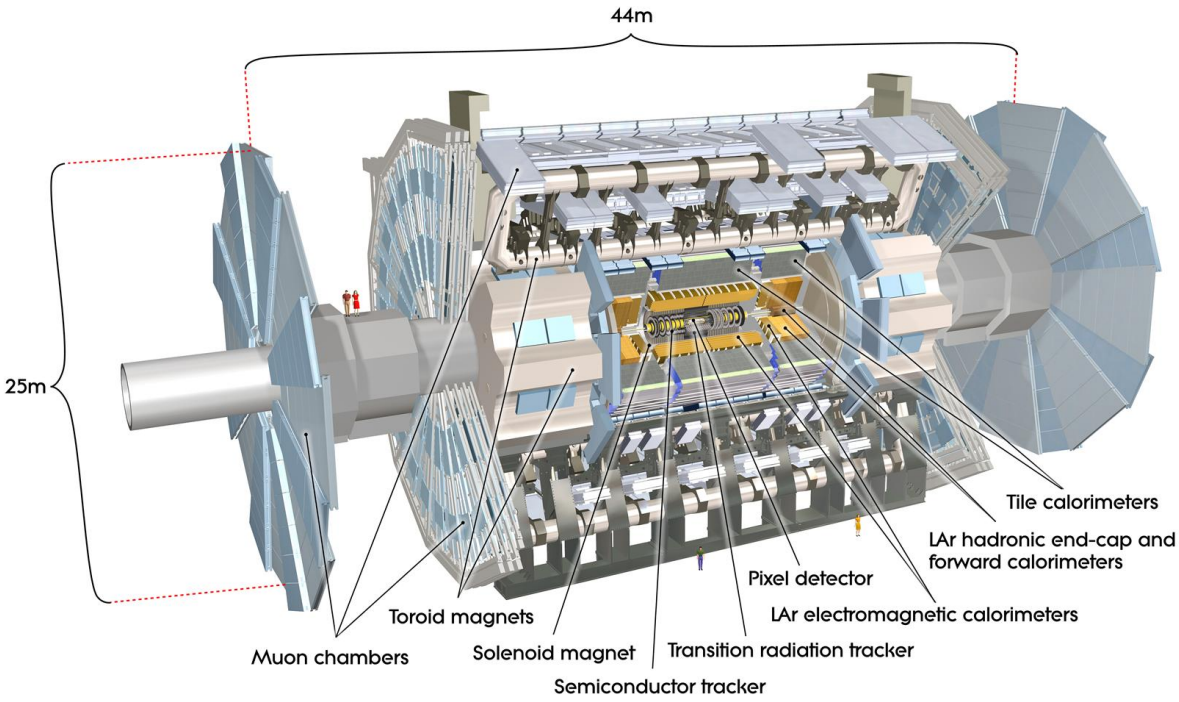
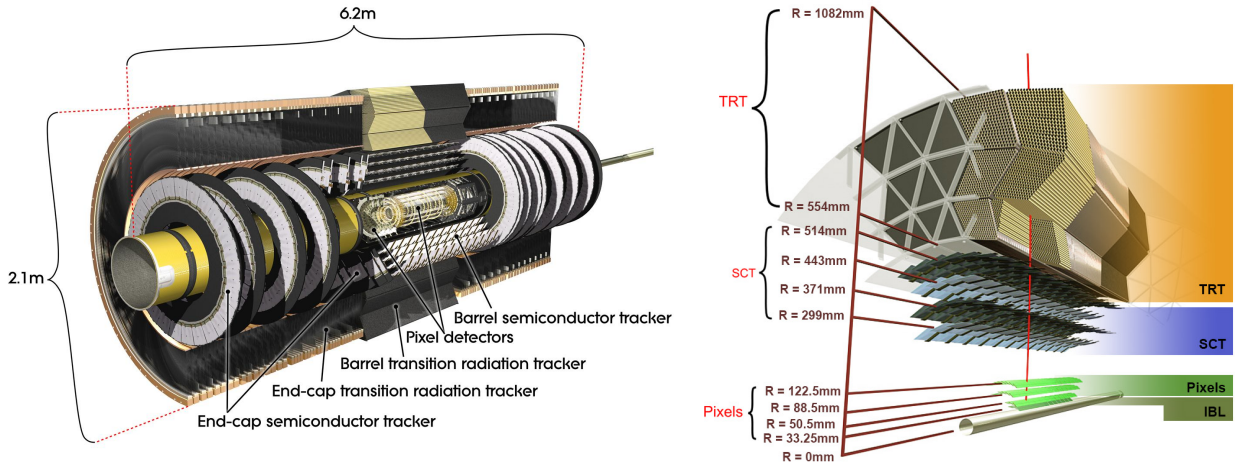


Figure 1.2: An illustration of the ATLAS detector [2].

The ATLAS experiment utilizes the ATLAS detector shown in Fig. 1.2, which is a 44-m-long and 25-m-wide detector. In order to search for answers to unexplained

physics phenomena in particle physics, the ATLAS detector is used to reconstruct particles generated through the proton-proton collisions.

Closest to the collision point lies the Inner Tracker System of the ATLAS detector shown in Fig. 1.3, which is used to measure the trajectory of charged particles in order to determine their momentum.



(**a**) Overall view of the Inner Tracker [3]. (**b**) Cross sectional view [2].

Figure 1.3: An illustration of the inner tracker of the ATLAS detector.

The Inner Tracker System consists of four main detector sub-systems: the Insertable B-layer (IBL), Pixel Detector System, the Semiconductor Tracker (SCT), and the Transition Radiation Tracker (TRT). The IBL is closest to the LHC beams[1], and was installed in 2013 in order to increase the performance of the inner tracking system [4]. The pixel detector system surrounds the IBL, and consists of 1,744 pixel modules with each having a 19×63 mm^2 surface area. Each module consists of 50×400 μm^2 sized pixels which can track particles to a 10 μm$\times 115$ μm resolution.

The semiconductor tracker consists of 4,088 modules which have silicon micro-strips used for tracking particles[2]. The transition radiation tracker (TRT) has 50,000 straw tubes in a barrel.

Surrounding the inner tracker system is a superconducting solenoid magnet that generates a uniform 2-T magnetic field for the tracking system. This magnetic field is

[1] More information regarding the IBL and the inner tracker system can be found in Appendix A.
[2] Each module has microstrips on both sides.

used to bend charged particles to measure their momentum.

Outside the solenoid magnet lie the Liquid Argon Calorimeters (LAr) and Tile Hadronic Calorimeters. The LAr calorimeters are electromagnetic calorimeters, which measures the energy of photons and electrons. The hadronic calorimeters are used to sample the energy of hadrons such as pions. These calorimeters are able to stop most particles, except for muons and neutrinos.

The momentum of muons cannot be measured with sufficient precision at very high momentum (order of TeV), by only using the Inner Tracker System [5]. Hence, there are dedicated torroidal magnets[3] which are used to bend muons towards the final layer of the ATLAS detector, the Muon Spectrometers, made from 4,000 individual muon chambers.

1.1.3 The physics goals of the ATLAS experiment

All particles excluding the Higgs boson, which were predicted by the standard model of particle physics, were detected by experiments prior to the LHC and the ATLAS experiment. Hence, one of the main goals of the ATLAS experiment when it started in 2008 was to search for the standard model Higgs boson. The ATLAS experiment, together with the CMS experiment succeeded in discovering the Higgs particle in 2012.

However, there are still several physical phenomena which cannot be answered by the standard model alone. Some examples are the existence of dark matter, imbalance in the particle-antiparticle numbers, and the hierarchy problem[4]. There are several "beyond the standard model" (BSM) theories which give theoretical answers to these unanswered physical phenomena, and one popular model is Super-Symmetry (SUSY). In SUSY, a super-symmetric partner exists for all standard model particles. However, their production and decay are rare processes, and more statistics is needed if we hope to detect them above the standard model background.

In addition to the search for new physics, detailed studies of the Higgs pair production and further experimental measurements of the Higgs boson properties also require an increase in statistics [6]. With these goals, the current LHC will be upgraded to the high luminosity LHC as described in the next section.

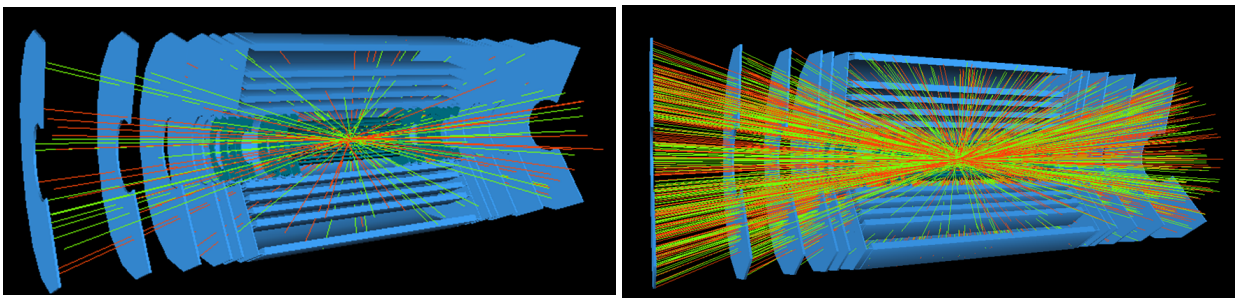
[3]These are superconducting magnets which can deliver a peak magnetic field of 4-T.

[4]The hierarchy problem refers to the relatively small mass of the discovered Higgs boson.

1.2 HL-LHC and upgrade of the ATLAS experiment

1.2.1 High Luminosity LHC and ATLAS upgrade project

The luminosity is proportional to the number of collisions, and this is important when it comes to increasing statistics needed for physics analyses (like rare processes). For this purpose, the LHC will be upgraded to the High Luminosity LHC (HL-LHC) by 2027, with the objective of increasing the luminosity roughly by a factor of 10 [7, 8].



(**a**) A pile-up of 23 events - Before (**b**) A pile-up of 230 events - After

Figure 1.4: An example of a simulation of the pile-up of collision events in the ATLAS inner tracker, before and after upgrading to the HL-LHC [9].

Due to the increase in luminosity, the number of collision events will be increased, as shown in Fig. 1.4. For the ATLAS detector, this means that the radiation damage will increase for different sub-detector systems (especially the inner tracker system), and the amount of data recorded per second will increase. Hence, the upgrade of the ATLAS detector is also ongoing simultaneously with the upgrade of the LHC to HL-LHC.

1.2.2 The new inner tracker system of the ATLAS experiment

One of the sub-detectors to be upgraded in the ATLAS detector is the inner tracker system, shown in Fig. 1.3. This whole inner tracker system will be replaced by the new one shown in Fig. 1.5.

Two types of pixel detectors are being developed for the new inner tracker system, as illustrated in Fig. 1.6. The innermost part is composed of pixel detectors having three

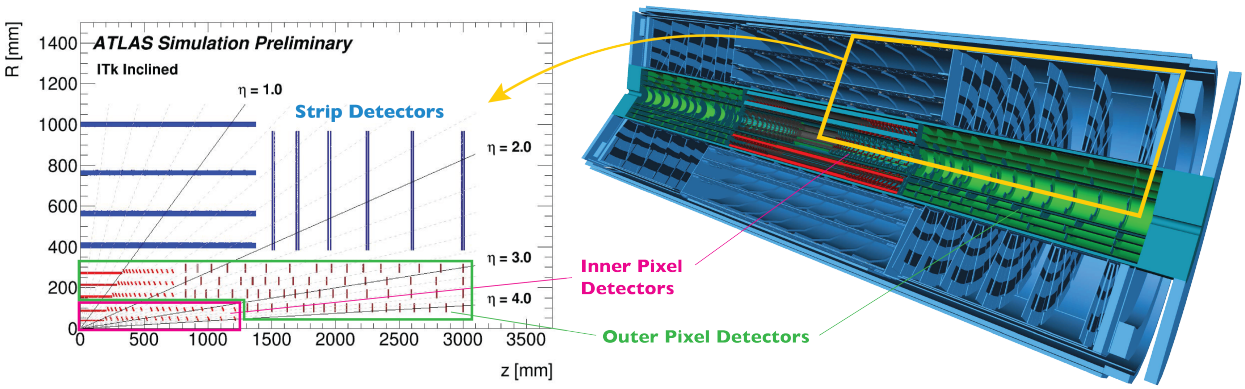


Figure 1.5: The new inner tracker system of the ATLAS detector for HL-LHC [10].

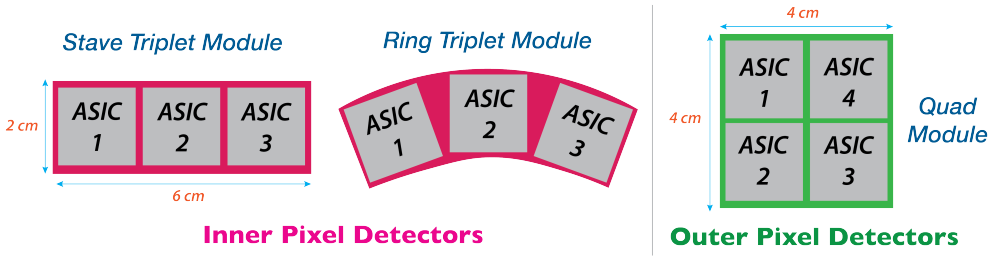


Figure 1.6: The types of pixel detectors proposed for the new inner tracker system.

ASIC[5] chips (known as Triplet Modules), while the outer part is composed detectors having four ASIC chips (known as Quad Modules). The pixel module or pixel detector mentioned in this thesis refers to these Quad Modules.

1.2.3 The new pixel detectors for the ATLAS experiment

Figure 1.7 shows the illustration of the prototype of Quad Modules. The new Quad Module consists of a silicon sensor which has pixel sizes of $50\ \mu$m$\times 50\ \mu$m, and can track particles to a resolution of $14\ \mu$m$\times 14\ \mu$m. There are 800 rows and 800 columns of pixels, which give a total of 640,000 pixels in one 4 cm$\times$4 cm pixel module. Four custom ASIC (Application Specific Integrated Circuit) chips[6] which process analog signals from the

[5]ASIC (Application Specific Integrated Circuits) will be discussed in more detail in the following sections, and chapters.

[6]The prototype pixel detectors mentioned in this research use the prototype RD53A ASIC [11].

silicon sensor and convert them to digital signals, are bump-bonded to this silicon sensor. The four ASIC chips are then wire-bonded to a Flexible PCB.

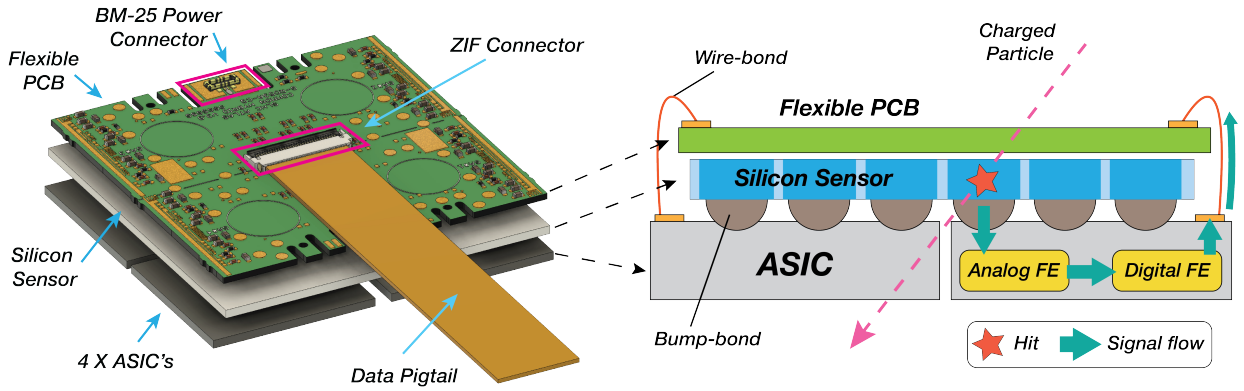


Figure 1.7: Left: 3-D illustration of the prototype quad pixel module, known as the RD53A Quad Module. Right: The cross-section of the pixel modules, showing the flow of hit and data signals.

Charged particles traversing the silicon sensor will excite electron and hole pairs in a pixel. These charges then move towards the bump-bonds due to the high voltage applied to the sensor, and induce a charge current in the bump-bonds, which flows into ASIC. In the ASIC, the analog front-end[7] will amplify and digitize the signals, and the digital front-end will serialize the signals at high speeds (1.28 Gbps). They are then first transmitted to a flexible PCB through the wire-bonds. The flexible PCB has a ZIF (zero insertion force) connector to which a flexible cable (referred to as the data pigtail) is connected. Through this flexible cable, the data signals can be transmitted to the downstream data acquisition (DAQ) system discussed in Section 1.3.3.

The flexible PCB also has a power connector[8] which carries the low voltage (LV) power from external power sources to the ASIC chips, and high voltage (HV) to the silicon sensor.

[7]The analog front-end contains a charge sensitive amplifier and a comparator. The amplifier will amplify charge signals and convert them into analog voltage signals. These will then get fed into the comparator which converts the analog signal into a digital signal.

[8]For the prototype pixel module, this is a BM-25 power connector.

1.3 Mass production of the new pixel detectors

The new pixel detector system will be composed of 10,000 pixel modules. Out of these, 2,000 of the outer pixel detectors (Quad Modules) will be produced in Japan. This section discusses the timeline of this production, and quality assurance - quality control (QA-QC) of the pixel modules.

1.3.1 The production plan

The production of the pixel modules in Japan will take place mainly in KEK, the Japan High Energy Accelerator Research Organization. The time line of the production since 2019 is shown in Fig. 1.8.

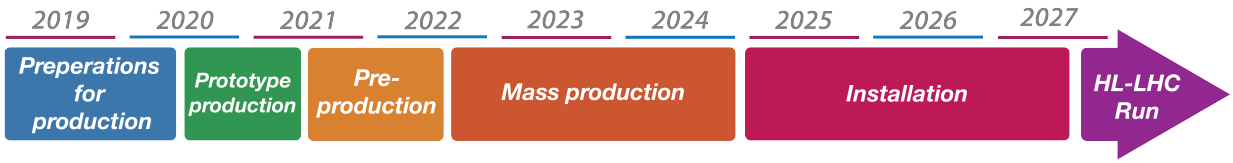


Figure 1.8: The time line for pixel module production in Japan.

Till the summer of 2020, the Japan group was focused on preparing for production and testing of pixel modules. From July 2020, the first prototype pixel modules were produced and tested in order to verify their performance.

The pre-production phase is scheduled to start in mid 2021. Here, a production and testing run of the actual pixel modules will be done to demonstrate the capabilities of the production sites in Japan. After this, the pixel modules will be mass produced in two and a half years.

Once the pixel modules are produced, they will be installed in the ATLAS detector during the long shutdown period from 2025 to 2027.

1.3.2 QA-QC and testing of pixel detectors

It is essential to ensure that the pixel modules which are installed in the new ATLAS inner tracker have a reliable performance. Hence, during the mass production of pixel modules, there is a detailed quality assurance and quality control (QA-QC) procedure for each pixel module.

A main part of the QA-QC procedure will include tests for checking the performance of the ASIC chips. Because the performance of ASIC is vital in certifying the quality of data coming from the pixel modules, the ASIC is verified as explained below. After verifying the ASIC, the same setup can be used to verify the performance of the silicon sensor, and the quality of the bump-bonds.

Testing the ASIC

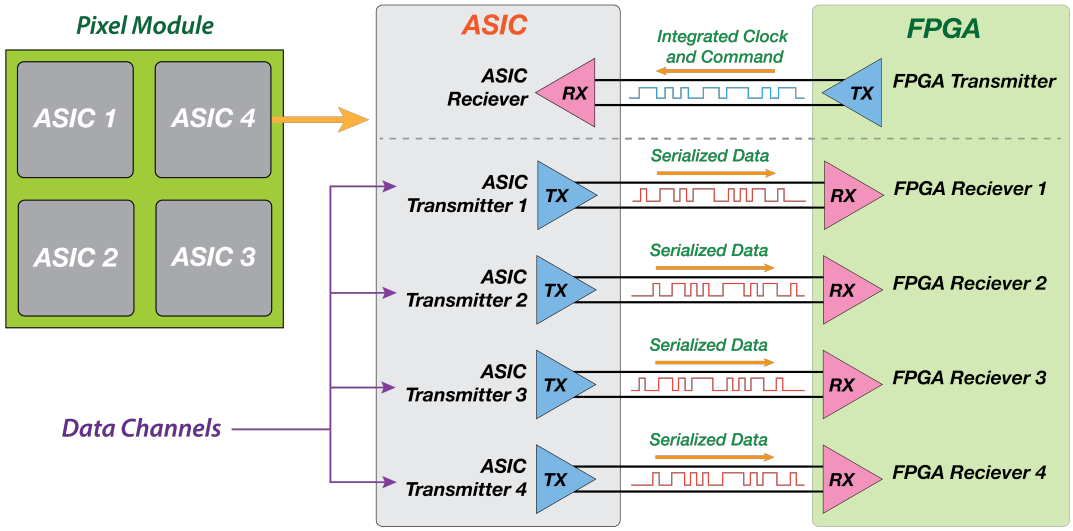


Figure 1.9: The signal transmission between the ASIC and the FPGA. Note that the ASIC can transmit signals in 4 channels at max.

To test the ASIC performance, first the ASIC needs to be programmed with configuration values needed for testing the different parts (the analog front-end and digital front-end). This is done by sending a command signal integrated with a clock signal from a FPGA[9] (field programmable gate array) transmitter (TX) to the ASIC receiver (RX). The FPGA is embedded on a FPGA development board, which is located far away from the pixel module, as described in Section 1.3.3.

After the ASIC is programmed, the serialized data is sent from the ASIC transmitters to the FPGA receivers. Because the data needs to be transmitted at high speeds, the data will be split into a maximum of four data channels when transmitting from the ASIC.

[9]FPGA's are used in testing because they are the best choice for customizing the transmitter and receiver needed for communicating with the custom ASIC.

1.3.3 The DAQ setup used for testing pixel modules

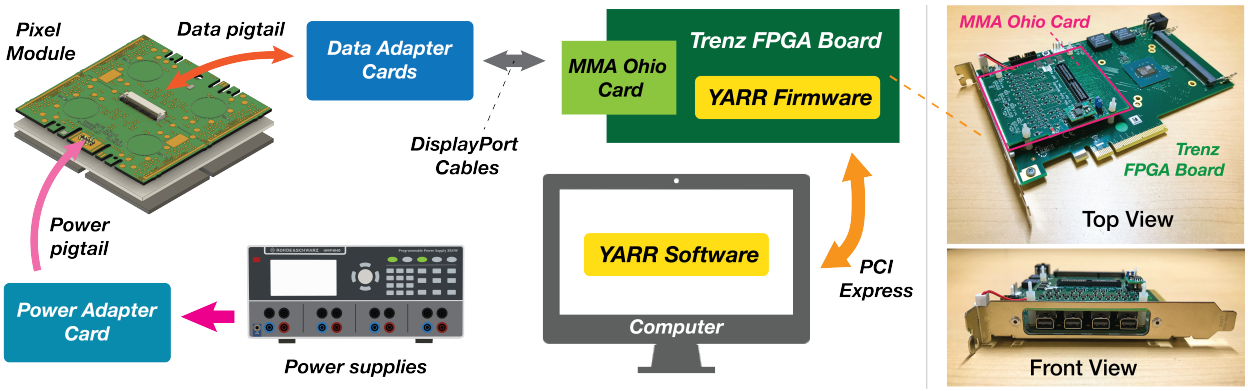


Figure 1.10: Left: An illustration of the flow of data through the DAQ setup. Right: The MMA Ohio card plugged to the Trenz FPGA board.

The data acquisition (DAQ) setup used for testing the pixel modules will include several components as shown in Fig. 1.10.

A commercially available FPGA development board, the Trenz FPGA board [12], is chosen for this DAQ setup. To connect multiple pixel modules to this FPGA board, a multi-module adapter (MMA) card designed by Ohio-State University[10] is used.

The MMA Ohio card has DisplayPort connectors as interfaces for connecting pixel modules, as shown in Fig. 1.10. However, the pixel modules use ZIF connectors as explained in Section 1.2.3. Due to this inconsistency, an adapter card was needed to route the signals coming from a ZIF connector to a DisplayPort connector. This adapter card is referred to as a data adapter card, and is explained in detail in Chapter 2.

The power for pixel modules need to be supplied through the power connector[11], as explained in Section 1.2.3. Hence, another adapter card which will carry the HV and LV power from power supplies to the pixel modules via a flexible cable (known as the power pigtail) is needed. This is referred to as the power adapter card, and is discussed in detail in Chapter 3.

In addition to the hardware components described above, a computer is needed in

[10]This is known as the MMA Ohio Card. This can be plugged directly into the FPGA through the FMC connector slots available on the Trenz FPGA board.

[11]For prototype pixel modules, this is a BM-25 connector

order to operate the Trenz FPGA board [12]. Also, the DAQ is based on a framework known as YARR (Yet Another Rapid Readout) [13] which is composed of two parts.

- The YARR Software - This is installed on the computer, and has all the software features needed to generate configuration files to program the pixel module ASIC chips.
- The YARR Firmware - This is programmed onto the FPGA chip, which is located on the FPGA board. The firmware will create a custom circuit on the FPGA, which includes a transmitter and a receiver needed to communicate with the ASIC.

1.4 The research objectives

The DAQ system which is used in testing pixel modules during mass production needs to be developed in stages. This is to ensure that the developed DAQ system is reliable and has no issues, so it can be used to assure and control the quality of pixel modules[13]. This system was first developed for testing the prototype pixel modules, and it will be improved in the coming years to the final DAQ system used during mass production.

The research discussed in this thesis has three main objectives.

1. The development of adapter cards (discussed in the previous section) for the prototype pixel modules, and verifying their performance.
2. The verification of the DAQ setup used for testing the prototype pixel modules in order to confirm that it is suitable for assuring and controlling the quality of pixel modules.
3. The verification of the performance of the ASIC of the first prototype pixel modules in the world.

Chapters 2 and 3 in this thesis discuss the development of adapter cards, and Chapter 4 discuss the verification of the DAQ setup simultaneously with the verification of the prototype pixel modules. Finally, Chapter 5 will state the conclusion of this research.

[12] Which is connected to the computer motherboard via the PCI express interface.

[13] In other words, the DAQ system should avoid issues like data corruption while transmitting data, since this would wrongly assume the pixel modules being faulty.

Chapter 2

Development of data adapter cards for pixel module testing

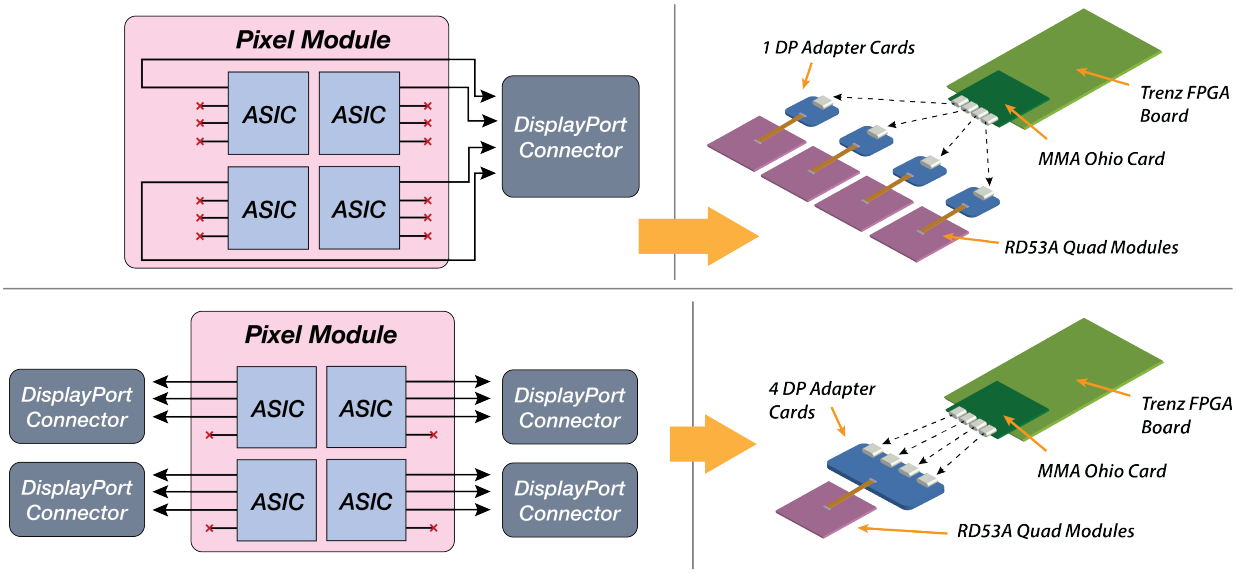


Figure 2.1: The two different topologies of data adapter cards.

It was discussed in Section 1.3.3 that data adapter cards were needed as an interface to connect the pixel modules to the downstream DAQ system. For these data adapter cards, two options shown in Fig. 2.1 were considered.

One option was to use only one data channel per ASIC, and route them to a DisplayPort

connector[1]. This way, one pixel module can be operated through one DisplayPort. Because the MMA Ohio card has four DisplayPorts, a total of four pixel modules can be operated at the same time[2], as shown in Fig. 2.1. The interface for this topology is called the **1-DisplayPort data adapter card**.

The other option considered was to route three data channels from one ASIC to one DisplayPort connector. This way, only one pixel module can be operated[3], as shown in Fig. 2.1, and this requires an interface with four DisplayPort connectors. Hence, this interface is called the **4-DisplayPort data adapter card**. This option has the benefit of reading out data at higher rates from the pixel module, compared to the 1-DisplayPort data adapter card[4].

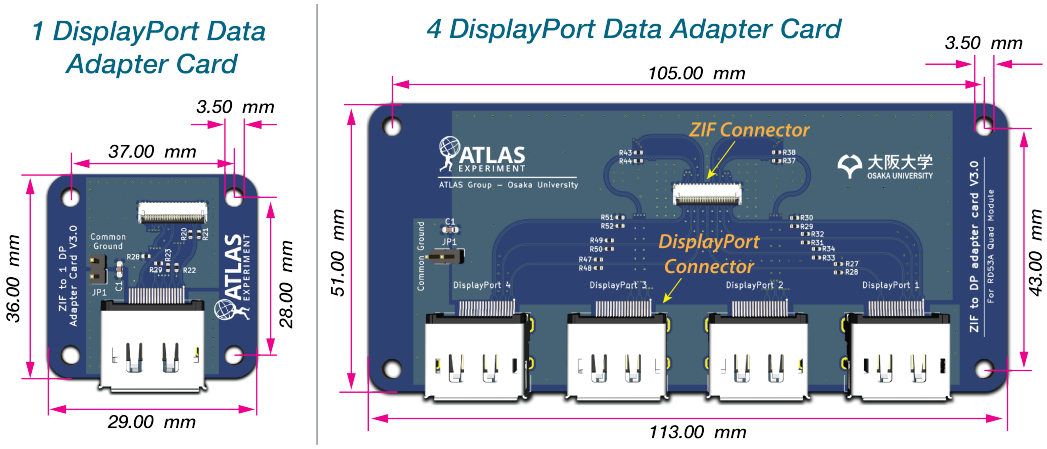


Figure 2.2: The two types of data adapter cards.

Figure 2.2 shows the two types of data adapter cards which I designed[5], in order to route signals from the ZIF connector to the DisplayPort connector(s). More information on adapter cards can be found in Appendix D.

[1]DisplayPort is a digital display interface, and supports differential signalling. The DisplayPort connector is used at the MMA Ohio card. Hence it was used for the Data Adapter Cards so it can be connected to the MMA Ohio card through a DisplayPort cable.

[2]This is known as the 16×1 topology, and this topology stands for 16 ASIC chips through 1 data channel per ASIC. A detailed discussion of the connection between data lanes can be found in Section 2.2.

[3]This is known as the 4×4 topology, and it originally stands for 4 ASIC chips through 4 lanes.

[4]Because it uses 3 data channels per ASIC. However, this is not the only reason. For the 1-DisplayPort data adapter card, if that one data channel in the ASIC has a problem, then we cannot read any information from the ASIC. However, for the 4 DisplayPort data adapter card, we can enable-disable data channels to find which one is causing the problem, and use the good ones to read data from the ASIC.

[5]All adapter cards were designed using the open-source EDA software KiCAD [14].

2.1 Pre-design considerations for the data adapter cards

The command (CMD) and clock (CLK) signals for the pixel modules are transmitted at 160 Mbps from the FPGA transmitter to the ASIC receiver[6]. Data can be transmitted at speeds 160 Mbps, 640 Mbps or 1.28 Gbps from the pixel module ASIC chips to the FPGA, over the DAQ setup shown in Fig. 1.10.

For this high speed data transfer between the ASIC and the FPGA, differential signalling is used. Hence, each data channel (including the CMD/CLK signals) from the ASIC to the FPGA, and vice-vera, use two differential lanes for signal transmission.

Further, the differential lane impedance of these data channels from the ASIC are controlled to 100 Ω. This requires that differential lanes on data adapter cards should have an impedance of 100 Ω, to avoid reflections of signals when they traverse the data adapter cards.

2.1.1 The layer stack-up

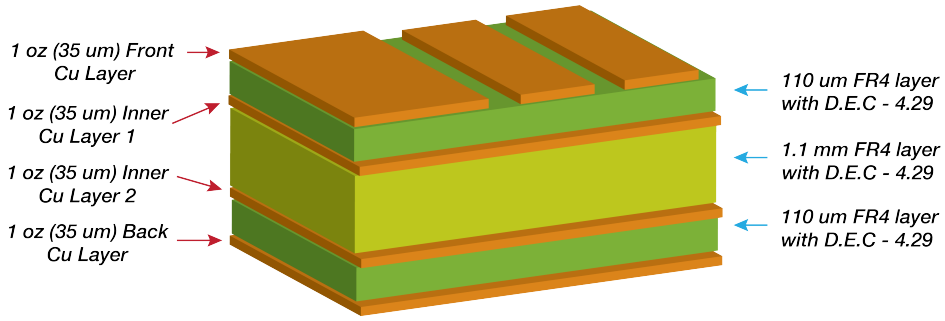


Figure 2.3: The layer stack-up for data adapter cards [15]. Here D.E.C stands for Di-electric Constant, and FR4 is the di-electric material supporting the copper layers.

It is important to include a reference ground layer under the signal traces [16] for differential signals. This is to control the differential impedance to 100 Ω, and for the return current to flow through[7]. The distance between the signal layer and the reference

[6]This process was illustrated in Fig. 1.9 of Section 1.3.2.

[7]Ideally the return current of one of the differential pairs flow through the other. But due to the coupling with the ground plane (which is essential to control the impedance), there will be a return current on the the ground plane as well.

ground should be small in order to control the impedance to 100 Ω. In addition to this, at least two planes for data transmission is needed to route signal traces so that they do not cross each other[8]. Hence, the 4 layer stack-up with two data transmission planes (the 1st layer and the 4th layer), shown in Fig. 2.3, is considered for the data adapter cards.

2.1.2 The calculation of trace impedance

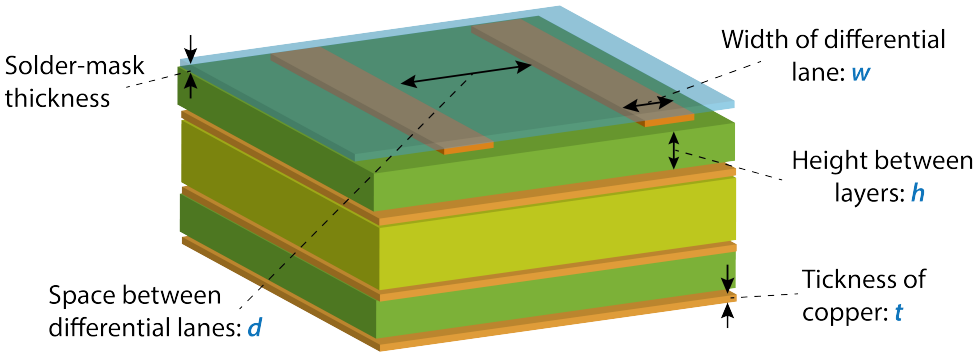


Figure 2.4: An illustration of the the PCB parameters which are needed to determine the differential impedance.

Practically it is difficult to achieve exactly 100 Ω impedance during production, due to the uncertainty of parameters that determine impedance. Hence, the standard is to calculate the differential impedance to a tolerance of $\pm$ 10% [16].

The suitable parameters for PCB traces for achieving the 100 $\pm$ 10 Ω differential impedance were determined by [17]:

$$Z_d = \frac{174}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)\left(1 - 0.48\exp\left(-0.96\frac{d}{h}\right)\right) , \tag{2.1}$$

where d is the space between differential lanes and w is the width of a differential lane. These parameters are illustrated in Fig. 2.4. The thickness of copper t, the height between layers h, and di-electric constant of the material ε_r are decided by the chosen layer stack-up discussed in Section 2.1.1. For these parameters, Equation 2.1 is expressed as:

$$100 = \frac{174}{\sqrt{4.29 + 1.41}} \ln\left(\frac{822.25}{w + 28}\right)\left(1 - 0.48\exp\left(0.00873d\right)\right) . \tag{2.2}$$

[8]This is explained in detail in Section 2.2.

A trace width w of 4 mils (101.6 μm)[9] and gap between traces d of 6 mils (101.6 μm) were chosen as integral values in mil units, and this gives 109.9 Ω according to Equation 2.2.

In actual PCBs, there is a solder resist covering the signal traces of the top and bottom copper layers. This solder resist has a different di-electric constant from the FR4 material, and will contribute to increasing the effective di-electric constant of Equation 2.1. Hence, using the determined width w and gap between traces d, the differential impedance was re-calculated with the contribution from the solder resist.

The recalculation was done using a software tool developed by Sierra Circuits [18], to handle the complexity of including the solder resist contribution. A trace width w of 4 mils and the gap between traces d of 6 mils gives a differential impedance of 106 Ω [10]. The impedance value 106 Ω satisfies the requirement for tolerance of $\pm$ 10 Ω, and hence, the above trace parameters were used for the data adapter card design.

2.1.3 The simulation of via parameters

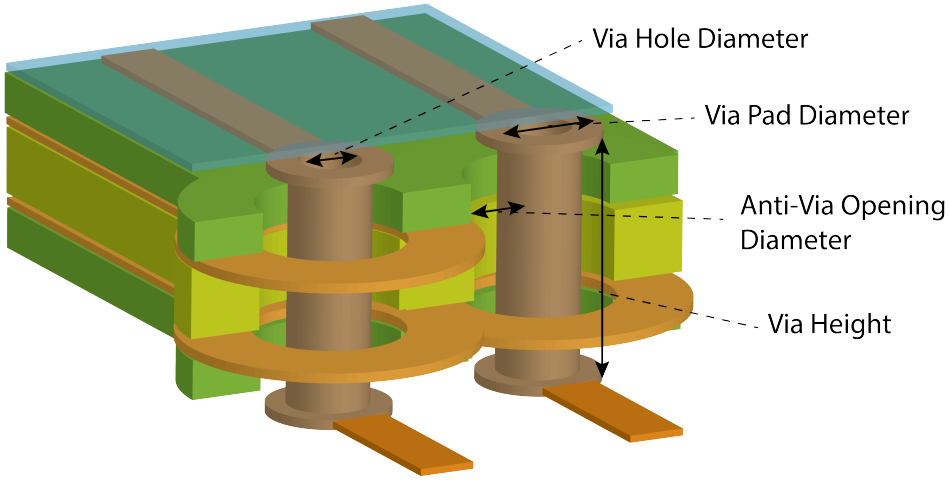


Figure 2.5: An illustration of the the PCB parameters which needed to determine the impedance of PTH vias.

Some of the data lanes needed to be routed on both the top and bottom layers of the

[9] 1 mil = 25.4 μm

[10] The results are mentioned in Appendix B. As mentioned earlier, the w and d parameters were set to be integers in mil units, and impedance cannot be controlled to exactly 100 Ω, due to the uncertainty in PCB parameters. Hence, the impedance is calculated such that it falls inside the $\pm$ 10 Ω tolerance.

data adapter card. These data lanes are connected with plated through-hole (PTH) vias as illustrated in Fig. 2.5. Hence, it was necessary to control the impedance of the PTH vias so that it matches the trace impedance.

Using the parameters determined in Section 2.1.2, the single ended impedance for signal traces was calculated to be about 63 Ω. Hence, the PTH via impedance was calculated to match this. The calculation was done using the Saturn PCB Toolkit Version 7.13 [19], and the following parameters were determined for the PTH vias[11].

- Via hole diameter: 0.2 mm.
- Via pad diameter: 0.4 mm.
- Anti-via opening diameter: 0.8 mm.

A key limitation of this calculation is the neglect of coupling between two PTH vias. For differential signals, the PTH via parameters should be determined to match the differential impedance, not the single ended impedance.

However, through testing with data adapter cards as explained in Section 2.3 and Chapter 4, there was no negative influence observed on the data transmission quality. This validated that neglecting the coupling between two PHT vias was allowable for the data adapter card design.

[11] The calculation result is shown in Fig. B.2 of Appendix B.

2.2 Design of the data adapter cards

As discussed in the introduction to this section, two versions of data adapter cards were required as interfaces between the pixel module and the FPGA, and these will route the data lines coming from the ZIF connector to the DisplayPort connectors as shown in Fig. 2.6. The flexible PCB and the four ASIC chips are shown. The orientation of the ASIC chips on a pixel module, and how the pixel module is connected to the data adapter cards are also shown.

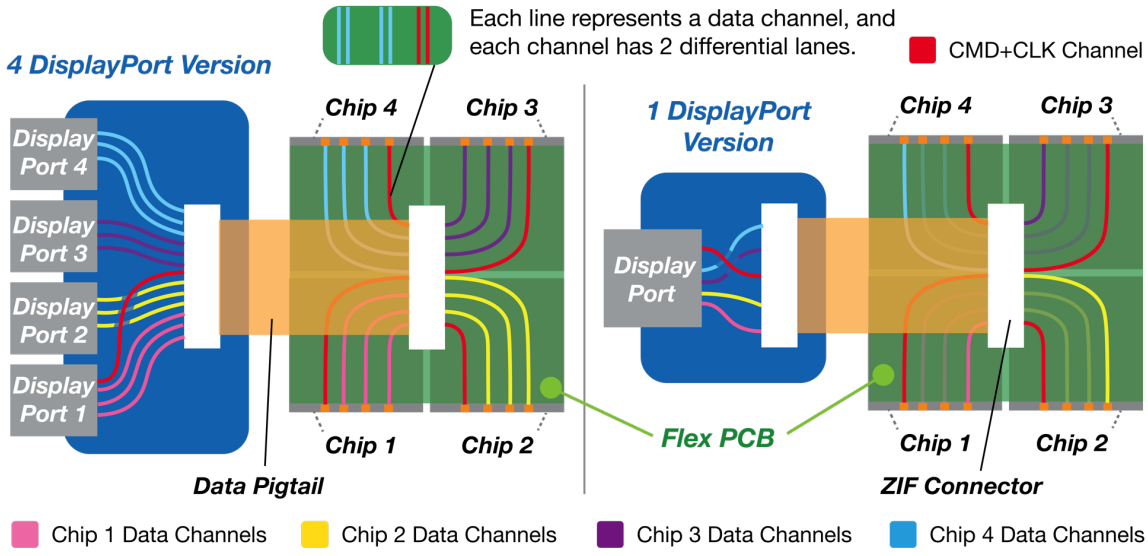


Figure 2.6: The connection of data channels from the pixel module to the data adapter cards. The 4-DisplayPort version uses three channels to read data from each ASIC chip, and the 1-DisplayPort version uses just one channel to read data from each ASIC chip.

A pair of differential lanes are referred to as a data channel. The 4-DisplayPort version can be used to read an ASIC chip through three data channels, and the 1-DisplayPort version can be used to read data from each ASIC chip through one data channel. The command (CMD) and clock (CLK) signals for all four ASIC chips is sent from just one channel from the FPGA to the pixel module, as illustrated in Fig. 2.7. This command and clock signals are split into 4 channels on the flexible PCB.
Table 2.1 shows the detailed connection of the data lanes to the DisplayPort lanes.

The schematics of the 4-DisplayPort and 1-DisplayPort versions of data adapter cards

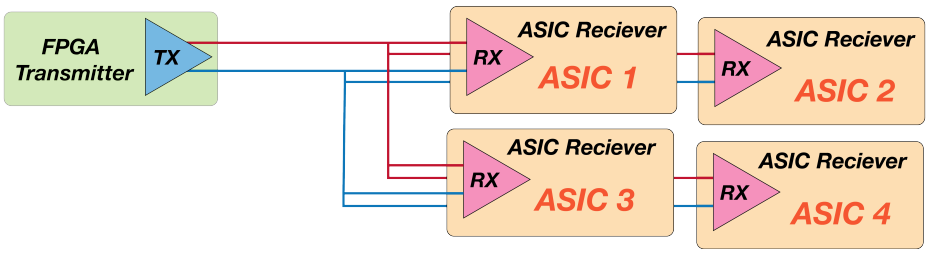


Figure 2.7: An illustration showing how the CMD/CLK signal is split into the 4 ASIC chips.

ASIC Chip	Channel	4 DP Card Lanes	1 DP Card Lanes
All chips	CMD/CLK channel	DP 1 aux. Channel	DP aux. Channel
Chip 1	Data channel 0	DP 1 data channel 0	DP data channel 0
	Data channel 1	DP 1 data channel 1	-
	Data channel 2	DP 1 data channel 2	-
Chip 2	Data channel 0	DP 2 data channel 0	DP data channel 0
	Data channel 1	DP 2 data channel 1	-
	Data channel 2	DP 2 data channel 2	-
Chip 3	Data channel 0	DP 3 data channel 0	DP data channel 0
	Data channel 3	DP 1 data channel 1	-
	Data channel 2	DP 3 data channel 2	-
Chip 4	Data channel 0	DP 4 data channel 0	DP data channel 0
	Data channel 4	DP 1 data channel 1	-
	Data channel 2	DP 4 data channel 2	-

Table 2.1: The mapping of data lanes from the pixel module, to the DisplayPorts (DP) of the data adapter cards.

can be found in Appendix D. The footprints which were designed using these schematics are shown in Fig. 2.8. The techniques 1 to 4 in Fig. 2.8 refer to several improvisations

and design techniques that were made when designing the data adapter cards, which are discussed in this section.

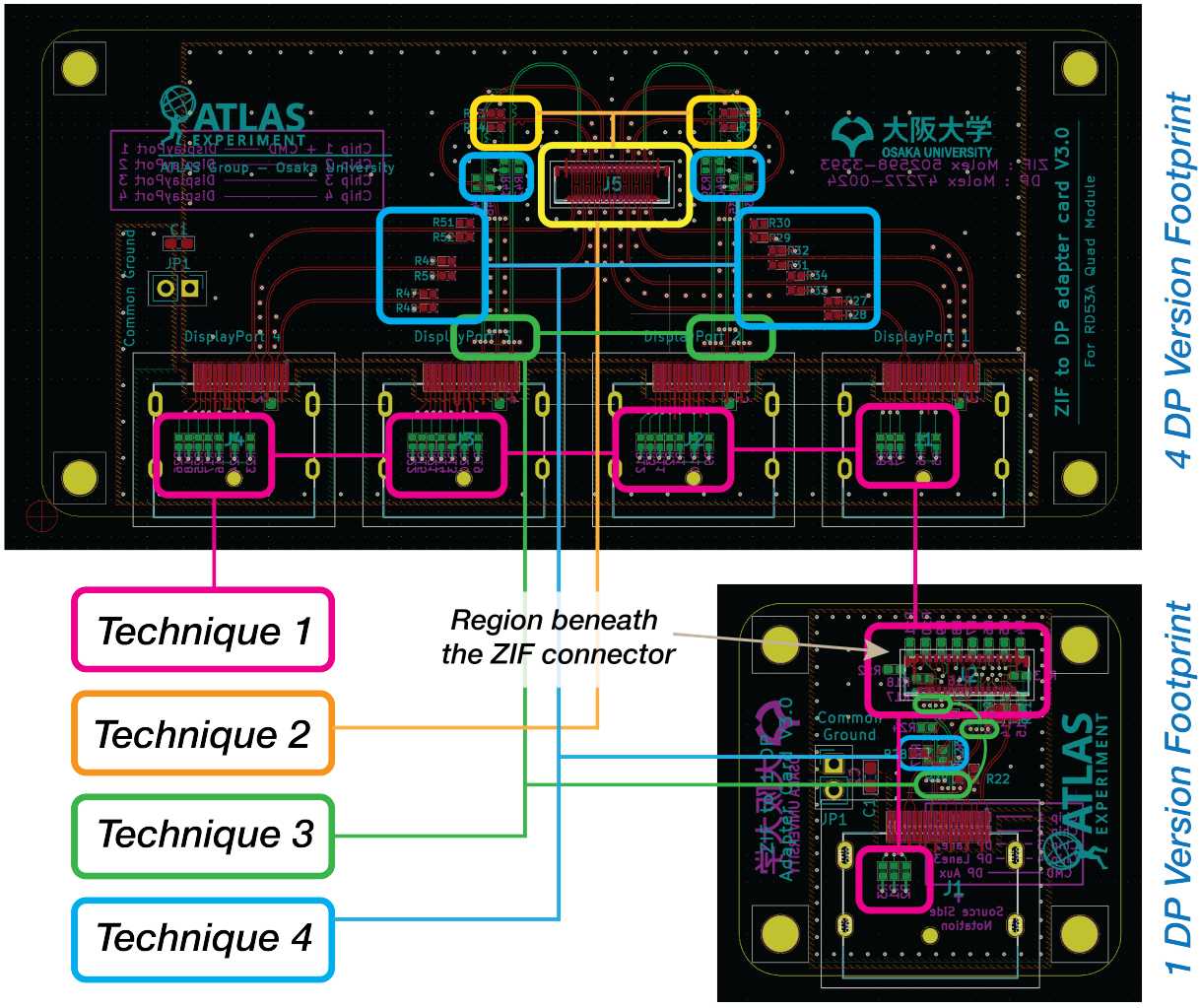
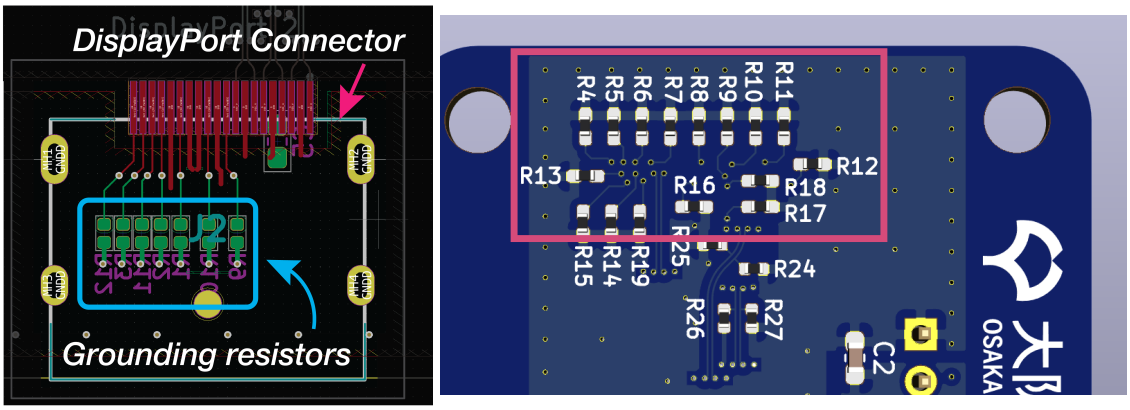


Figure 2.8: The footprint of the 4-DisplayPort data adapter card and the 1-DisplayPort data adapter card.

2.2.1 Technique 1: Grounding unused signal lanes

A DisplayPort connector has 20 pins, as shown in Fig. 2.9(a). However, only eight pins are used at maximum[12] for sending and receiving data, and seven pins are always grounded. This will result five or seven pins not being used. If these pins are left floating, cross-talk due to coupling of signals in the DisplayPort cable[13] will get reflected back into the FPGA receiver. Hence, the unused data lanes were grounded using 50 Ω resistors as shown in Fig. 2.9(a). This is equivalent to a half of the differential impedance of the data lanes.



(a) (b)

Figure 2.9: a) The grounded resistors on the 4 DP Data Adapter Card. b) The region denoted by a pink box is beneath the ZIF connector of the 1 DP data adapter card, and consists of 50 Ω resistors to ground the unused data lines.

A similar feature for the 1-DisplayPort data adapter card is in the region beneath the ZIF connector shown in Fig. 2.8. An enlarged image of the 3D model of this region is shown in Fig. 2.9(b). As shown in Fig. 2.6, the 1 DP data adapter card only uses 4 data channels, out of the total 12 channels routed to the ZIF connector. Due to this, the unused lanes are left floating on the data pigtail and cross-talk signals can get reflected back to the pixel module. To avoid this, there are resistor pads in the region shown in pink in Fig. 2.9(b), which can be soldered by 50 Ω resistors to terminate these lines to ground.

[12]DisplayPort-1 has three data channels and the CLK/CMD channnel, and each channel has two data lanes. For other DisplayPort connectors, there are only three data channels.

[13]An explanation on cross-talk is done in Appendix C.

2.2.2 Technique 2: Length equalizing of differential pairs

For differential signalling, positive and negative going signals are transmitted at the same phase from a transmitter, and their difference is taken at the receiver. If the lengths of differential lanes in each pair are not made equal, it will cause a difference in phase between the positive and negative signals, and deform the differential signal as shown in Fig. 2.11.

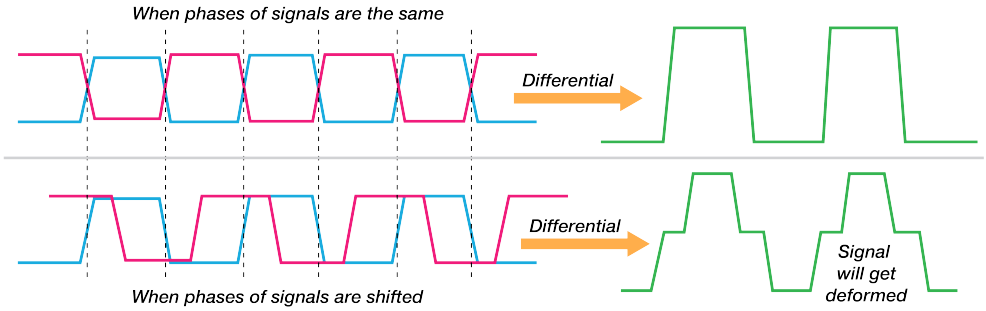


Figure 2.11: When the phases of differential signals differ, the signals will be deformed when taking their difference.

In addition, if signals are in the same phase, the noise due to electromagnetic interference (EMI) can be cancelled off by taking their difference[14]. This is another advantage for using differential signalling. In other words, a shift in phase will make the differential signals more prone to EMI noise.

For a signal traversing a PCB, the propagation speed can be calculated by [20]:

$$v = \frac{c}{\sqrt{0.475 \cdot \epsilon_r + 0.67}} = \frac{3 \times 10^8}{\sqrt{0.475 \times 4.29 + 0.67}} = 1.82 \times 10^8 \,\mathrm{ms}^{-1}\,, \tag{2.3}$$

where ϵ_r is the di-electric constant of the PCB material. A 1.28 Gbps signal transmits a bit in 0.78125 ns. Hence, the length corresponding to 1 bit signal in a PCB is $0.78125\,\mathrm{ns} \times 18.2\,\mathrm{cm\,ns}^{-1} \sim 14\,\mathrm{cm}$. This shows that even a 1.4 cm difference between signals can cause a 10% distortion of the differential signal.

The differential pair of one data channel will come from pads on opposite sides of the ZIF connector, as shown in Fig. 2.12. This is to make sure that differential pairs in a data

[14] If the two signals are $+V$ and $-V$, and a noise ΔV is added, then the difference is $V_d = (V + \Delta V) - (-V + \Delta V) = 2V$.

channel stay next to each other on the data pigtail, as illustrated in Fig. 2.13.

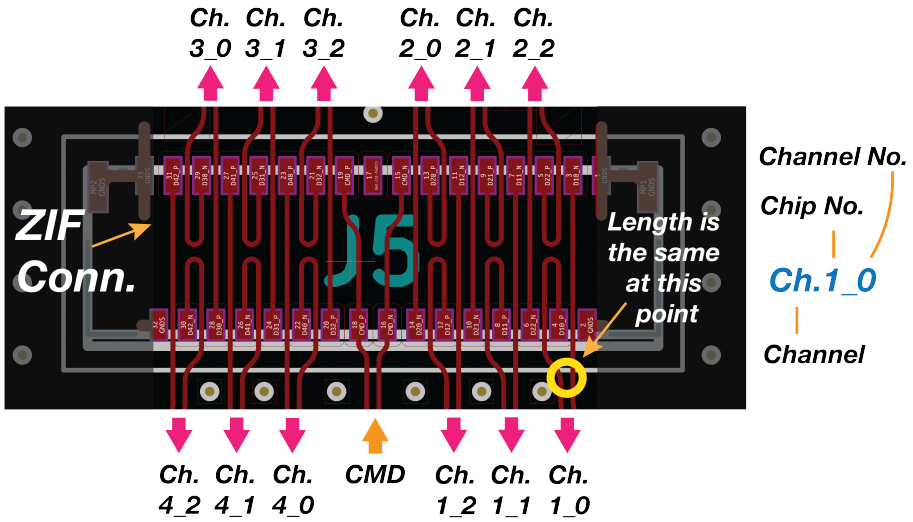


Figure 2.12: How length of differential lane pairs are adjusted under the ZIF connector. Blue color is a different data channel from the yellow colored one.

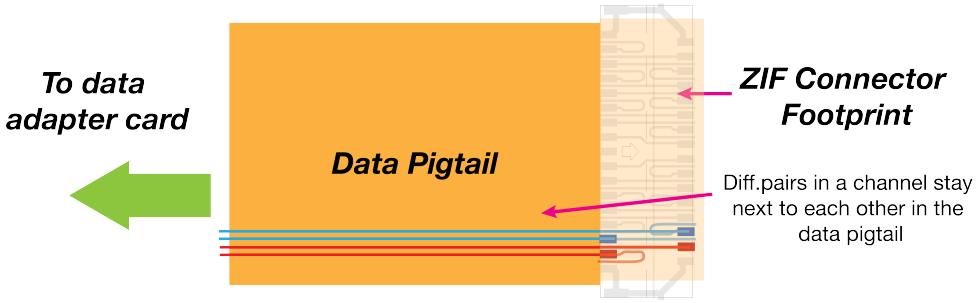


Figure 2.13: The differential pairs in a data channel are routed to the ZIF connector such that each pair stays next to each other on the data pigtail.

On the data adapter card, if differential pairs are routed in straight lines from the pads, the differential pair will have different lengths at the point depicted by a yellow circle in Fig. 2.12. On the flexible PCB design for the pixel module, the same mismatch of length exists at the ZIF connector. Furthermore, some lanes on the data adapter card had to be routed as shown in Fig. 2.14, which added more mismatch in length.

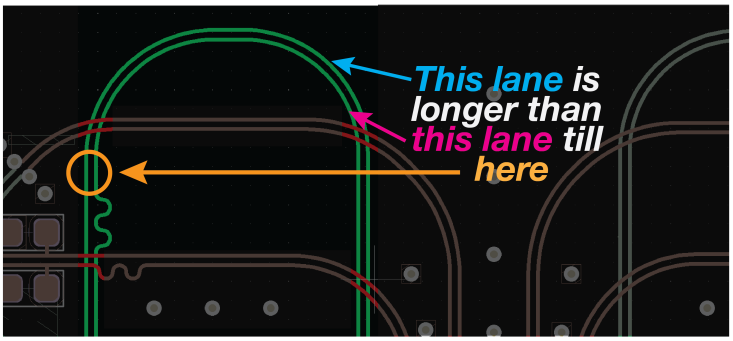


Figure 2.14: The data channels for Chip 2 and Chip 3 had to be routed like shown, since they are taken from the opposite side of the ZIF connector, as can be seen from Figures 2.12 and 2.8. After the point shown in a yellow circle, the length is adjusted by using a serpentine delay line.

This mismatch in length is estimated to be on the order of 1 cm. Compared to the previous calculation result from Equation 2.3, it was considered necessary to equalize the length of data lanes on the data adapter card, to avoid a large shift in phase between differential signals.

To minimise this phase shift, first the lengths were equalized immediately after the signals come out of the ZIF connector. Hence, by routing as shown in Fig. 2.12, the length was equalized at the point depicted by a yellow circle. This method was adopted from the same improvisation done on the flexible PCB[15]. Secondly, the length mismatch of the differential pair shown in Fig. 2.14 is corrected by adding a serpentine delay line.

[15]Designed by Ilya Tsurin, Univeristy of Liverpool.

2.2.3 Technique 3: Vias for the return current

Due to routing of data lanes to the ZIF connector as shown in Fig. 2.6, it was challenging to route the channels from Chip 2 and Chip 3 on the 4-DisplayPort data adapter card. Also for the 1-DisplayPort data adapter card, lanes will overlap as shown in Fig. 2.6.

The solution was to route them to the back side of the adapter card, and then bring them to the front after crossing the obstacles (in this case, the data lanes of Chip 1 and Chip 4), through a pair of PTH vias as shown in Fig. 2.8.

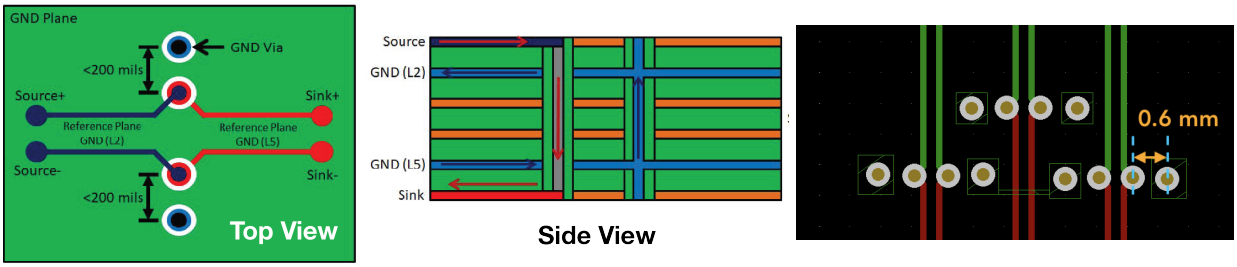


Figure 2.15: a) The recommended placement of return current vias, according to [16]. b) The placement of return current vias in the actual design.

Due to the parameters selected to control the differential impedance to $100 \pm 10\,\Omega$, the gap between the outer and inner layers[16] (110 μm) is less than the gap between the traces (152.4 μm). This means that there will be a considerable coupling between the signal layer and the reference ground layer, which will lead to a return current on the reference ground layer. Note that this is in addition to the return current on the differential lanes. For high speeds signals, this return current path is directly below the signal traces [21].

When high speed differential signals go through vias, there should be an equal set of vias for the return current on the reference ground plane to flow, from one reference ground plane to the other [16] [17]. This is illustrated in Fig. 2.15 and the vias for the return current were placed as close as possible to the signal vias.

[16] Outer layers are where signals traces are routed, and inner layers are for the reference ground.

[17] To put it simple, since the signals change layers, the reference ground plane for the signals should change as well.

2.2.4 Technique 4: High Ohmic resistors for grounding data lanes

The power for pixel modules installed in the ATLAS inner tracker is supplied through a serial powering chain, as illustrated in Fig. 2.16. The ASIC voltage regulator is explained later in Section 4.3.1

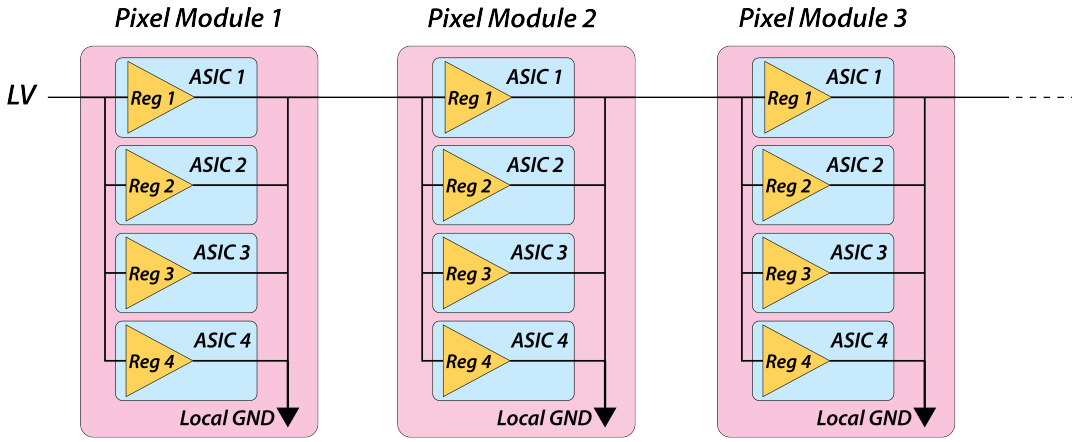


Figure 2.16: A serial powering chain is used to supply power to the pixel modules when installed in the ATLAS detector.

Due to this serial powering chain, the pixel modules will have different reference grounds (local grounds) caused by the voltage drop from the regulator in the ASIC.

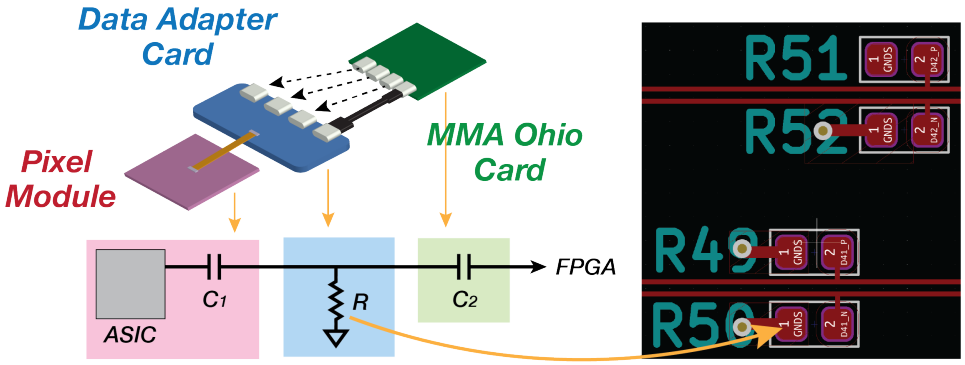


Figure 2.17: AC-coupled points shown on the simplified DAQ system. High Ohmic resistors are added to DC couple data lanes on the data adapter card.

The downstream DAQ setup, the MMA Ohio card and the FPGA, uses a common ground. If the data channels from the ASIC chips were connected directly to the downstream DAQ, it would create an imbalance of grounds between the modules. Due to this imbalance, current will pass through the MMA Ohio card ground, and could cause problems when operating MMA Ohio card and the FPGA.

For this powering chain to be initially tested for the ASIC, capacitors to AC-couple the data channels were added at the MMA Ohio Card. However, for the protoype pixel modules, the AC-coupling capacitors were added on the flexible PCB of the pixel module. This was to have them as close as possible to the ASIC transmitters. This would result in a double AC-coupling, one at the MMA Ohio card and one on the pixel module as shown in Fig. 2.17, and leave the data lines on the data adapter card floating. To avoid this, grounded high Ohmic resistors of 10 kΩ were added to the data lines as shown in Fig. 2.17. They were added as close as possible to the data lines, to minimize impedance mismatching at these points.

2.3 Validation tests of the data adapter cards

We produced the data adapter cards discussed in the previous section, and validated their performance through several tests listed below. These tests are discussed in detail in this section.

1. High speed readout at different data rates.
2. ZIF connector - patch cable mating cycles.
3. Patch cable length dependence.
4. Impedance measurement results of the data adapter card, together with the data pigtail and the pixel module Flexible PCB.

Tests 1-3 were done before the Quad Modules were produced, and a dedicated test setup shown in Fig. 2.18 was used.

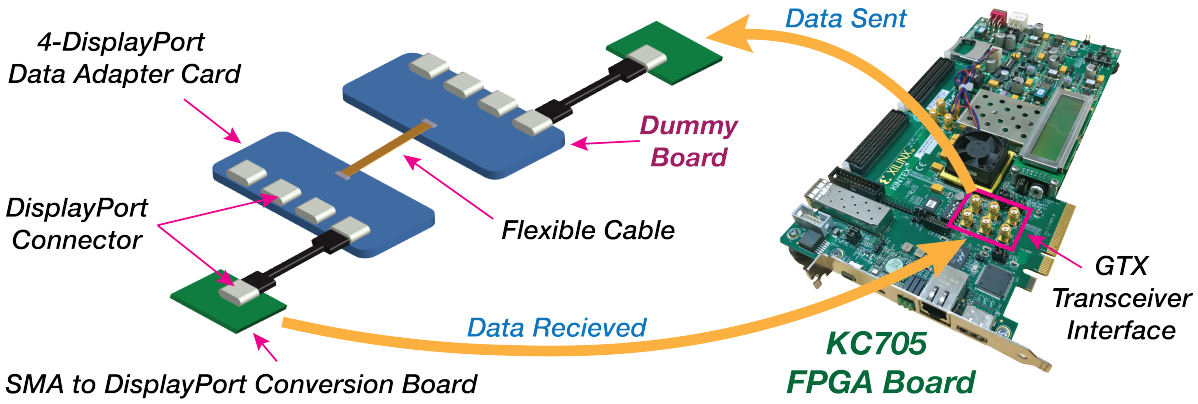


Figure 2.18: The dedicated test setup used for initial testing of data adapter cards.

The Dummy Board used in this test setup is an adapter card which has a mirrored routing of signals to the ZIF connector[18], compared with the 4-DisplayPort data adapter card. Therefore, it will have the same routing of signals as on the pixel module. For

[18]The lane mapping shown in Fig. 2.11 is mirrored at the center (at the CMD lane position). Hence, from bottom left to bottom right, it will be Chip-1-Channel-0, Chip-1-Channel-1 and so on. This is the same lane assignment at the ZIF connector on the flexible PCB.

verification of the data adapter card performances, this dummy board was used instead of the pixel module.

It was important to verify performance of the data adapter cards at several data rates, as discussed in Section 2.3.3. For this purpose, the gigabit transceivers (GTX) of Xilinx FPGA's [22] were the suitable candidates, since its data transmission speed can be configured between 500 Mbps and 12.5 Gbps.

The Xilinx FPGA development board used for this test was the KC705. On this board, the GTX of the FPGA are routed to SMA (Sub-Miniature version A) connectors. However, since the adapter cards use DisplayPort connectors, a SMA-DisplayPort conversion board was also required for this test, as shown in Fig. 2.18.

Before discussing the validation test results, the Integrated Bit Error Ratio Test (IBERT) which is used to validate the data adapter cards is discussed first.

2.3.1 Integrated bit error ratio test (IBERT)

The integrated bit error ratio test (IBERT) is used to evaluate the performance of a data transfer system which includes a data transmitter and a receiver, and the medium between the two [23]. Here, the bit error ratio (BER) is simply the ratio between the number of bit errors and the number of total bits transmitted.

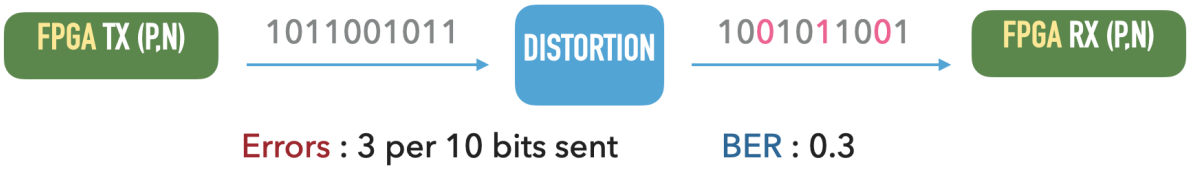


Figure 2.19: When a bit pattern is sent from the FPGA's transmitter (TX), some bits may get distorted as the bit pattern reaches the FPGA's receiver(RX). The bit error ratio is the ratio between these distorted bits to total bits sent.

As shown in the illustration of Fig. 2.19, bit errors occur due to distortions in the transmitting medium. This is unavoidable, and the best we can do is to improvise our setup such that it minimizes the bit error ratio.

The integrated bit error ratio test (IBERT) in Xilinx's Vivado software with the KC705 FPGA board was used to measure the bit errors when a bit pattern is sent through the

validation setup shown in Fig. 2.18. In the IBERT test, a feature called 2-D eye scan is used for analysing the performance of the DAQ system.

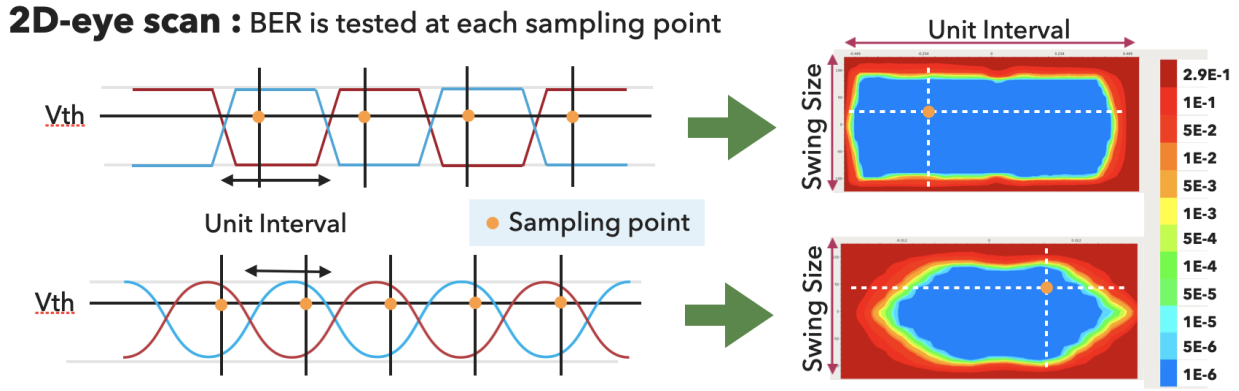


Figure 2.20: An illustration of how a 2D eye scan works.

In a 2D eye-scan, the bit error ratio is measured for each sampling point as shown in Fig. 2.20, and plotted in a 2D diagram. The X-axis for the diagram shows the unit interval for a signal, and the Y-axis shows the voltage value at the sampling point. The Y-axis can be taken as a measure of the signal's swing. The Z-axis shows the upper limit for the BER. As shown in Fig. 2.20, the more a signal is distorted, the higher the BER is at its boundary and beyond.

The blue region of the 2D eye-scan is where BER is the lowest[19]. This is called the open area of the eye, and the 2D eye scan gives a value to this area which is proportional to actual area of this region. By measuring how much this value varies to different transmission conditions, it can give a sense of the signal transmissions performance through a DAQ system.

2.3.2 Bit error rate (BER) calculations

The required upper limit of BER

As mentioned in the introduction, Japan will produce about 2000 pixel modules for the new ATLAS inner tracker system, and there will be dedicated QA-QC procedures to determine if pixel modules are faulty or not. Hence, we need to assure that not even one

[19]For the test results discussed in this thesis, if the bits were determined in this blue region, the bit error ratio (BER) was zero.

module is mistakenly considered to be faulty due to bit errors, regardless of the pixel module being actually faulty or not[20]. Hence, the probability of a module failing due to bit errors should be less than $1/2000$.

A pixel module has four ASIC chips, and each chip has 160,000 pixels[21]. Each pixel will be verified 100 times by injecting pulses to it (as discussed in Section 4.1.1). Also, each data frame sent by the ASIC is 66 bits long, and contains the information of eight pixels [11]. Therefore, the required upper limit of the bit error ratio (BER) can be calculated by following equation.

$$BER_{\,upper\ limit} = \frac{1}{2000\ (\text{No. of pixel modules})} \times \frac{1}{160000\ (\text{No. of pixels per ASIC})} \times \frac{1}{4\ (\text{No. of ASIC chips})} \times \frac{1}{100\ (\text{No. of digital injections})} \times \frac{8(\text{No. of pixels per data frame})}{66(\text{Data frame size})}\,. \tag{2.4}$$

Using Equation 2.4, the upper limit of bit error ratio is calculated to be,

$$BER_{\,upper\ limit} = \frac{1}{1,056,000,000,000\ \text{bits}} = 9.5 \times 10^{-13}\,.$$

Hence, the measured bit error ratio should be less than 9.5×10^{-13}.

The measured upper limit of BER at 95% confidence level

When zero bit errors are observed, the upper limit of the number of bit errors at a particular confidence level (C.L) can be set using Poisson statistics. The probability of getting x with the expectation value of μ for the Poisson distribution is,

$$P(x) = \frac{\mu^x\, e^{-\mu}}{x!}\,. \tag{2.5}$$

Hence, the probability of getting 0 for the Poisson distribution is,

$$P(0) = \frac{\mu^0\, e^{-\mu}}{0!} = e^{-\mu}\,. \tag{2.6}$$

[20]Since bit errors considered here happen on the data transfer system, and not the pixel module.

[21]The prototype ASIC has 76,800 pixels, but the final ASIC, which will be used for the mass produced pixel modules, has 160,000 pixels.

The upper limit on bit errors a, at the 95% confidence level with zero bit errors observed can be written as,

$$\int_0^a e^{-\mu}\, d\mu = 1 - e^{-a} = 0.95\,. \tag{2.7}$$

Hence,

$$e^{-a} = 1 - 0.95 = 0.05 \rightarrow a = 2.99 \sim 3 \text{ bit errors.} \tag{2.8}$$

This means that if zero bits errors are observed after transmitting N bits, the upper limit of bit errors at 95 % confidence level can be taken as 3 bits. Hence, the measured BER upper limit can be calculated as:

$$BER_{\text{measured upper limit}} = \frac{\text{Bit errors at 95\% C.L}}{\text{Total bits transmitted}} = \frac{3 \text{ bit errors}}{\text{Total bits transmitted}}\,. \tag{2.9}$$

2.3.3 High speed readout at different data rates

This test was done to ensure that the data adapter card was able to transmit data at 1.28 Gbps without significant attenuation of signals. For evaluation between different data rates, the Integrated Bit Error Ratio Test (IBERT) and the 2D eye-scan mentioned in Section 2.3.1 were used.

Data Rate	Passed/Total Channels
1.56 Gbps	12/12
3.125 Gbps	12/12
6.25 Gbps	10/12

Table 2.2: BER result at different data speeds

The BER was measured for five minutes (to achieve more than 10^{11} transmitted bits) at three different data speeds: 1.56 Gbps, 3.125 Gbps and 6.25 Gbps, for all 12 data channels[22]. If the bit error ratio (BER) is less than 10^{-9} for a specific channel, it is marked as **Passed**. Table 2.2 shows the result for this test. It should be noted that at 6.25 Gbps, the 10 channels

[22]reminder - a pair of differential lanes are referred to as a data channel

which passed show zero bit errors, while the failed channels showed more than 10^4 bit errors.

To visualize the above result, the 2D eye scan was taken for the different data rates. Fig. 2.21 shows the result of the 2D eye scan for a specific channel.

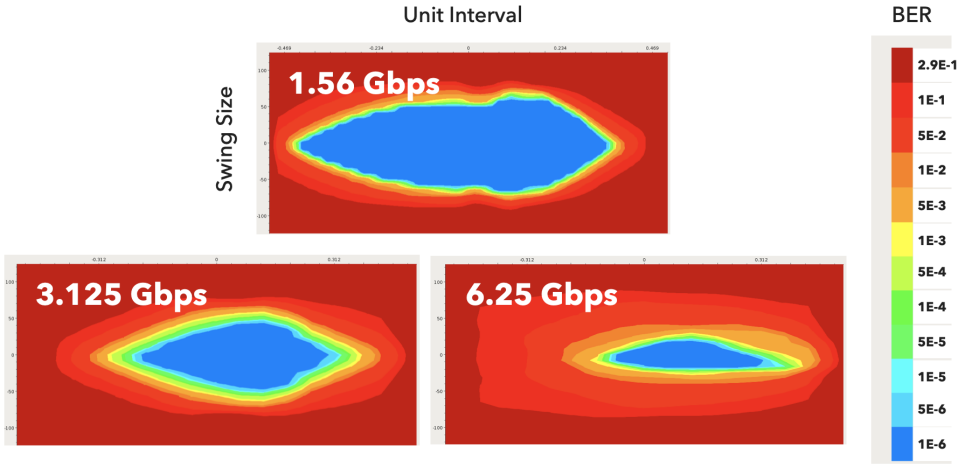


Figure 2.21: The test result of the IBERT 2D eye-scan for different data rates.

The eye region is smaller at higher data transfer rates. For 6.25 Gbps, the open area of the eye is extremely small. A slight variation of data lane parameters [23] may distort the signal to the point that there is no perfect spot for zero bit errors. This was considered as the cause for the 2 failed channels at 6.25 Gbps. Hence, the maximum data transfer rate for all channels to pass is between 3.125 Gbps and 6.25 Gbps. However, it should be noted that several extra points where data attenuation and signal reflection are likely to occur (the SMA conversion board, the Dummy board and extra DisplayPort cables) do not exist in the real pixel module testing setup.

Even with these extra attenuation and signal reflections, data transfer for all 12 channels at 1.56 Gbps was possible without any bit errors, for a 24-hour measurement. This gives an upper-limit for the measured bit error ratio (using Equation 2.9) at the 95% confidence level as:

$$BER_{\text{measured upper limit}} = \frac{3}{1.56 \times 10^9 \times 3600 \times 24} = 2.2 \times 10^{-14}\,. \tag{2.10}$$

[23] This is not only for the data adapter cards, but for the whole setup shown in Fig. 2.18.

Comparing with the bit error ratio (BER) estimation done in Section 2.3.2, the measured upper limit is smaller than the required upper limit needed for pixel module testing. We concluded that the designed adapter card was able to transfer data at the maximum 1.28 Gbps without any bit errors, and they are usable for performing QA-QC of pixel modules.

2.3.4 ZIF connector - patch cable mating cycles

During quality assurance and quality control (QA-QC) of pixel modules, it is required to attach and detach the pixel modules from the data adapter card several times (on the order of 100). However, as specified in the data sheet for the ZIF connector [24], the maximum mating cycles is 10 in order to keep the contact resistance below 60 mΩ. Further, the maximum mating cycles for abrasion is given as 1000 cycles for the patch cable. Hence, this validation test was necessary to ensure that the impedance at the connection did not change significantly. If there was a significant change in impedance, then signals would be distorted more when travelling through the ZIF connector, and the open area of the 2D eye should decrease.

Figure 2.22 shows the results of one data channel at 3.125 Gbps, for 1000 mating cycles of the ZIF connector. For each mating cycle, an IBERT (for a few minutes) was done and the value of the open area of the 2D eye-scan was obtained.

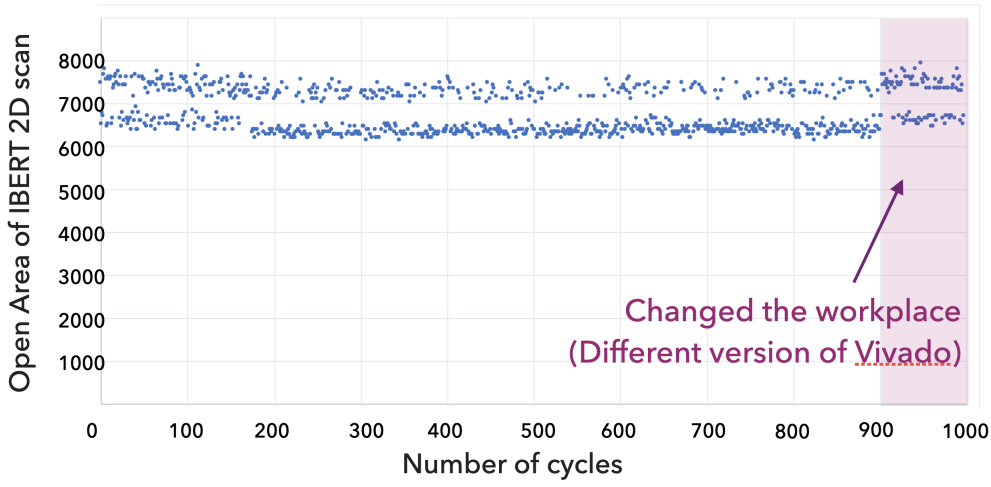


Figure 2.22: The result of the ZIF-patch cable mating cycles test.

The variation of the 2D eye-scan open area value is shown in the plotted data. The split of this open area into two bands is considered to be due to two reasons. The first is the discreteness of this open area measurement. Since measuring the voltage to re-create the size of the swing has a discreteness, the open area should also vary in discrete steps. The second reason is due to the connection between the ZIF connector and the data pigtail being slightly different each time it is mated. Due to this slight difference, if the swing of the signal changes, then open area value will be pushed to an upper band or lower band. The fluctuations on these bands are considered to be due to the small differences in unit interval measurement[24].

Between 900-1000 cycles, the test setup was moved to a new workplace and a new version of the Vivado software was used; it seems to have influenced the open area to be calculated slightly larger. However, this change did not influence the conclusion mentioned below.

Through this result, the open area does not change significantly even after 1000 mating cycles. Hence, we concluded that the possible change in contact resistance was not an issue for data transfer through the ZIF connector.

2.3.5 Patch cable length dependence

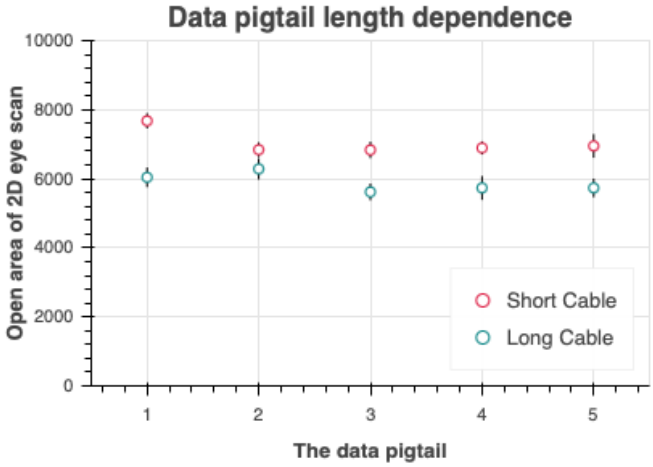


Figure 2.23: The result of the patch cable length dependence test.

[24]Since the FPGA uses a clock to sample each point in the unit interval, this process is also done in discrete steps.

For the QA-QC of pixel modules, we need to use different lengths of patch cables (referred to as data pigtails in the actual testing setup) depending on the testing setup. However, there is more signal distortion in longer cables.

To test this, five pieces each of two patch cables differing in length: 10.16 cm and 25.4 cm, were tested. Each cable was tested for 10 times using IBERT, and the average and standard deviation of the 2D eye-scan open area was obtained. The speed of data transfer used for this test was 3.125 Gbps.

The result of this test is shown in Fig. 2.23. The result shows that the longer patch cable has a smaller open-area, compared to the shorter one. This means that more signal distortion has occurred when signals travel a longer distance on the patch cable material. However, even with this distortion, the open area was large enough that bits could be correctly determined. Hence, we concluded that longer patch cables were also viable to be used for the DAQ system for connecting pixel modules to the data adapter card.

2.3.6 Impedance measurement of the DAQ system

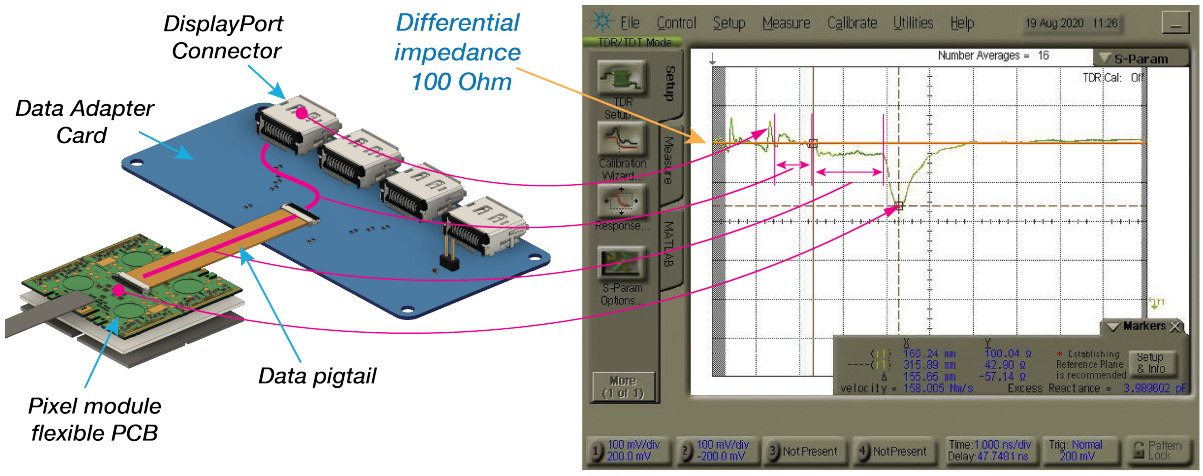


Figure 2.24: The TDR measurement results from SLAC, obtained from [25]. This measurement is for differential impedance of the CMD/CLK channel at 160 Mbps.

The impedances of data lanes on the 4-DisplayPort data adapter card, the data pigtail, and the pixel module flexible PCB, were measured by the ATLAS group at SLAC [25]. They have used time domain reflectrometry (TDR)[26] to determine the impedance.

The results of the TDR measurement for CMD/CLK channel are shown in Fig. 2.24. Here X axis is the distance in mm, and Y axis is the voltage which can be converted into differential impedance. The differential impedance of this data channel on the data adapter cards is well controlled to 100 Ω, which confirms that the pre-design considerations discussed in Section 2.1 were proper enough to control the differential impedance to 100 Ω.

However, the differential impedance of the CMD/CLK channel on the data pigtail was measured to be around 90 Ω, and this is seen to drop even more on the flexible PCB, the lowest being at 40 Ω. The reason for this large impedance mismatch on the flexible PCB is thought to be due to the choice of the layer stack-up[25], and the routing of CMD/CLK channel as explained in Section 2.2. This was recognized as a point to be improved, and the next version of the flexible PCBs for the pixel modules will include a reference ground layer in order to control the differential impedance more accurately to 100 Ω.

[25]This flexible PCB design has not used a reference ground layer, which makes it difficult to control the differential impedance

Chapter 3

Development of a power adapter card for pixel module testing

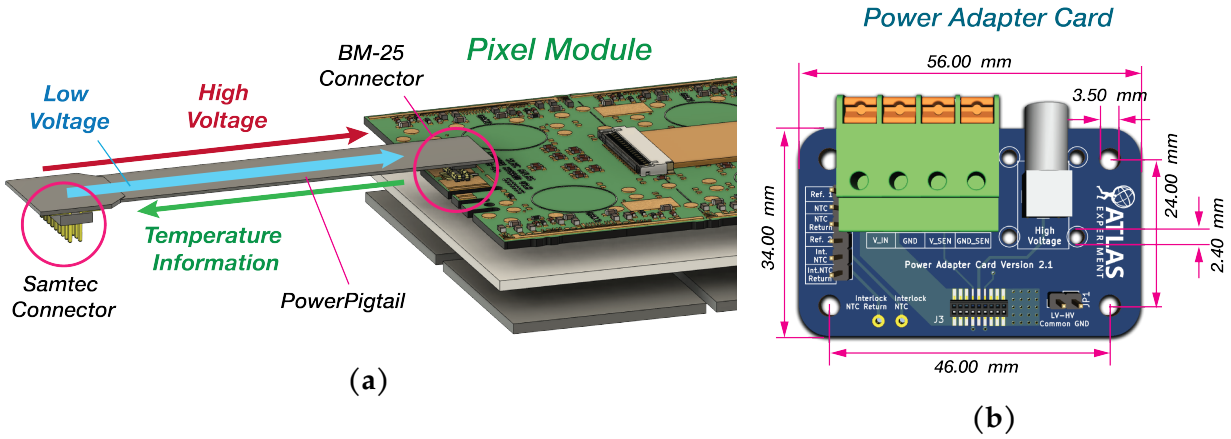


Figure 3.1: a) The requirements for the power adapter card. b) The power adapter card for testing pixel modules.

As discussed in Section 1.3.3, an interface card was needed to carry low voltage power and high voltage from the power supplies to the pixel modules. In addition to this, temperature information can be measured from the NTC thermistors[1] on the flexible PCB for the pixel module. All these are routed from the BM-25 connecter to a Samtec connector on the power pigtail, as shown in Fig. 3.1(a).

Hence, an interface card known as the power adapter card was developed, which

[1]Discussed in detail in Section 3.2.2.

satisfies all the functions described above. This chapter discuss the design and validation of this power adapter card.

3.1 Pre-design considerations for the Power Adapter Card

Higher resistance in powering chains will have joule heating. Since each pixel module ASIC operate at a maximum of 1.1 A constant current mode, a pixel module which consists of four ASIC chips require 4.4 A to operate. A pixel module operates at about 1.5 V, and hence generates about 6.6 W of heat. At 4.4 A, even a small resistance of 100 mΩ will give a 0.1 V voltage drop and 0.44 W of heat. This is around 7% of the heat generated in the system, and will be a burden on the cooling system used for the pixel module testing[2]. Hence, reducing even small resistances was an important consideration for the pixel module powering scheme.

3.1.1 PCB Parameters

For the power adapter card, lowering resistances could be achieved through changing the parameters of the traces. The resistance can be calculated as:

$$R = \frac{\rho \cdot L}{A} = \frac{\rho \cdot L}{W \cdot H}\,, \tag{3.1}$$

where A is the cross-sectional area of the copper traces, ρ is resistivity of the copper trace at 20 °C ($0.0171\,\Omega{\cdot}\mathrm{mm}^2{\cdot}\mathrm{m}^{-1}$), L is the length of the trace, W is the width of the trace, and H is the thickness of the trace. A conductor which carries current will increase its temperature due to joule heating. Incorporating the temperature rise, Equation 3.1 is modified as:

$$R = \frac{\rho \cdot L}{A} = \frac{\rho \cdot L}{W \cdot H} \cdot (1 + \alpha \cdot (T_{\mathrm{Overall}} - 20\ ^{\circ}\mathrm{C}))\,, \tag{3.2}$$

where $T_{\mathrm{Overall}} - 20\ ^{\circ}\mathrm{C} = \mathrm{T_{Rise}}$ is the maximum temperature rise given in [°C]. Here α is the resistivity temperature coefficient, and it is $3.9 \times 10^{-3}[^{\circ}\mathrm{C}^{-1}]$ for copper. The maximum current I_{Max} passing through the trace [27] is:

$$I_{Max} = (k \cdot T_{Rise}^{b}) \cdot A^{c} = (k \cdot T_{Rise}^{b}) \cdot (W \cdot H)^{c}\,, \tag{3.3}$$

[2]For example, some QA-QC procedures will require the pixel modules to be cooled down to -35 °C. Hence, extra sources of heat generation will be a burden when trying to cool down to really low temperatures.

where k, b and c are constants decided by a curve fitting for measured I and T [28], and they are $k = 0.048$, $b = 0.44$, and $c = 0.725$ for copper traces[3].

For the power adapter card, it is desirable to have less than a 10 °C increase in the trace temperature, to avoid any overburden on the cooling setup used for QA-QC as described before. The maximum current through the power adapter card is 4.4 A as mentioned previously, but 14 A is considered as an upper-limit for the PCB design (for safety reasons). This will give the $W \cdot H$ product in Equation 3.3 as:

$$(W \cdot H)^{0.725} = \frac{14}{0.048 \times 10^{0.44}} \rightarrow W \cdot H = 620.8[\text{mils}^2] = 0.401[\text{mm}^2] \,.$$

The copper thickness options were 1 oz/ft^2 (0.035 mm) or 2 oz/ft^2 (0.07 mm). Hence, the 2 oz/ft^2 (0.07 mm) option was chosen, giving $W = 5.7$ mm. Rounding this, a width of $W = 6$ mm was chosen[4] for the low voltage trace on the power adapter card.

[3]Here, W and H are given in mils, and unit conversion of 100 mil = 2.54 mm should be done.
[4]This gives an I_{Max} 14.5 A

3.1.2 Power connectors and power cables

The selection of power connectors was important for the powering scheme. The following connectors in Table 3.1 were selected due to the low contact resistances, and the ability to withstand power.

Connector	Type	Place	Function	Contact R
Hirose BM25-4S	FPC to Board connectors	Flex PCB	Connect to power pigtail	5 mΩ per pin
Hirose BM25-4P	FPC to Board connectors	Power Pigtail	Connect to flex PCB	5 mΩ per pin
Samtec FTM-109-02	SMT Micro Terminal Strips	Power pigtail	Connect to adapter card	15 mΩ per pin
Samtec CLM-109-02	Rugged Reliable Micro Sockets	Power adapter card	Connect to power pigtail	15 mΩ per pin
Phoenix Contact 1017505	Terminal Block	Power adapter card	Connect LV power cables	1.3 mΩ

Table 3.1: The different types of connectors used for the RD53A pixel module powering scheme. Here R stands for resistance, and the resistance values in this column are for maximum mated resistance per pin (except for the terminal block). Mated means when both the plug and the receptacle connectors are fixed to each other.

Further, the powering cables were selected so that the voltage drop in the cable is small as possible [29]. For the 4.4 A testing scheme, the recommendation was set to a 1.5 m AWG size 16 or thicker powering cables, in order to reduce the resistance in the wires. For a 1.5 m powering cable, this would lead to 19.8 mΩ and a voltage drop of 0.087 mV (at 4.4 A).

3.2 The design of the power adapter card

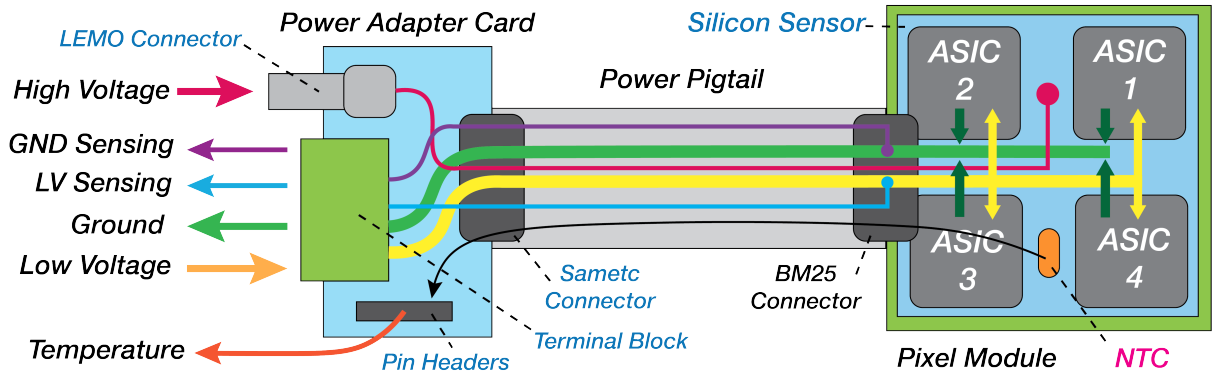


Figure 3.2: An overview of the power adapter card functions. GND refers to ground, and LV refers to low voltage.

The main task of the power adapter card is to supply low voltage power and high voltage to the pixel module. Low voltage power is supplied from the power supplies through the terminal block, and goes all the way to the pixel module flexible PCB. Here it will get routed to each ASIC. Each ASIC will take in the required amount of the current, and the return current is sent through the Ground terminal back to the power supply, as illustrated in Fig. 3.2.

At 4.4 A, since there is a relatively large voltage drop on the powering chain, the voltage on the power supply will be much higher than the actual voltage on the pixel module. Hence, two high impedance voltage sensing terminals are also added to measure the voltage at the BM-25 connectors.

The high voltage is supplied through a coaxial connector (LEMO connector), and goes to the flexible PCB where it gets routed to the silicon sensor. In addition to these functions, there is also a pin header referred to as the NTC readout block, to read the resistance values of NTC thermistors on the pixel module. Note that all of these are routed through the Samtec connectors and power pigtail, to the BM-25 connectors.

The schematics of the power adapter card can be found in Appendix D. Some details of the power adapter card and the powering scheme is discussed below.

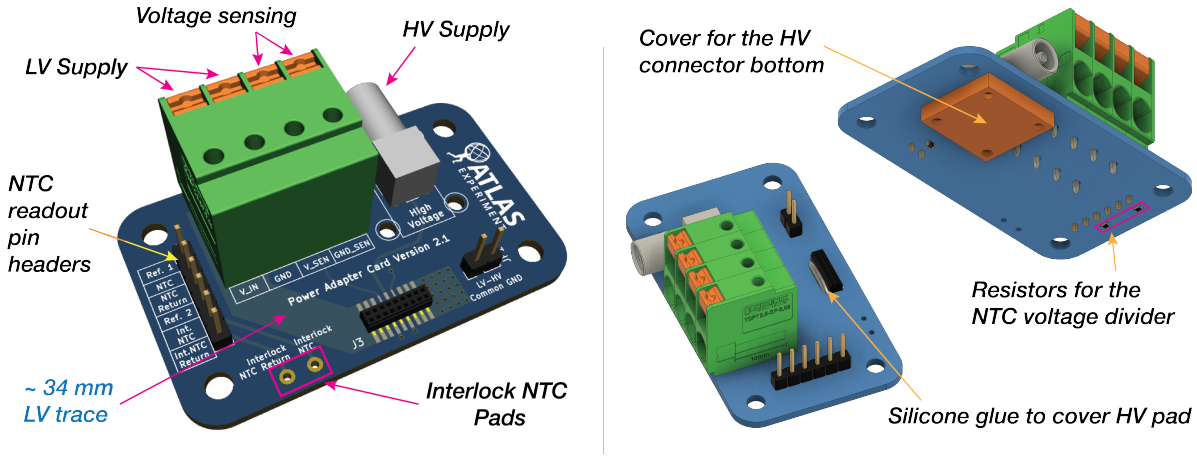


Figure 3.3: The 3D image of the power adapter card.

3.2.1 Low Voltage and High Voltage Supply

The low voltage is supplied by a **Rhode & Schwarz - HMP 4040** power supply[5] terminal block, shown in Fig. 3.4, directly to the terminal block of the power adapter card. This direct connection to the terminal block reduces the contact resistance [6] which can cause a large voltage drop.

The HMP4040 power supply has two voltage sensing terminals to which the voltage sensing terminals from the power adapter card can be connected. As explained before, these high impedance terminals can measure the actual voltage at the BM25 connector of the pixel module, and give feedback of to the power supply to compensate for the voltage drop.

The high voltage is supplied by a **Keithley 2410** power supply, which can generate up to 1100 V. This high voltage is supplied to the power adapter card through a LEMO connector, as explained in the introduction to this section. Since the HV pin underneath the LEMO connector and the Samtec connector pad which carries the HV were exposed, there was a risk of electrocution if these pads were accidentally touched. To avoid this, a 3D printed cover for the LEMO connector, and silicone glue on the Samtec connector pads were added.

[5]This is the recommended power supply, but some institutes use different power supplies as well.

[6]If we use banana connectors for example, it will cause a larger voltage drop in the powering chain, due to the larger contact resistance.

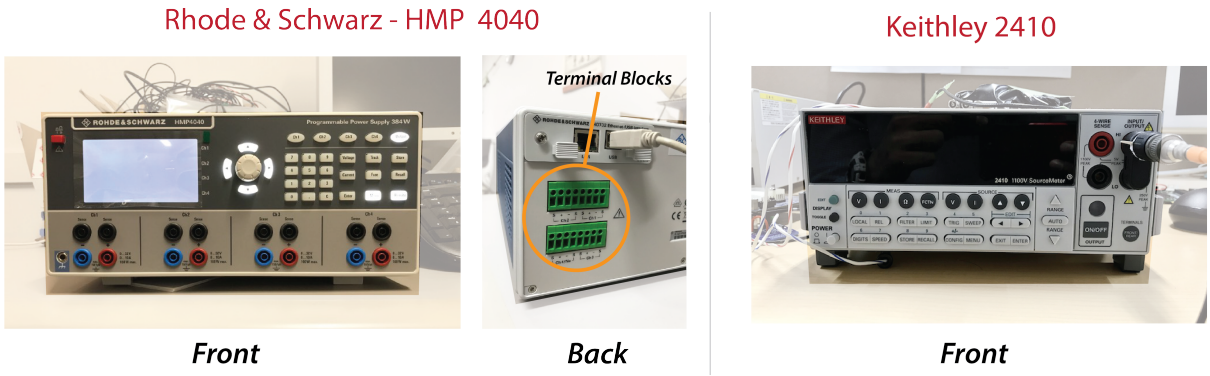


Figure 3.4: The power supplies used for Low Voltage (HMP 4040) and High Voltage (Keithley 2410).

3.2.2 NTC thermistor readout block

The power adapter card will also have a feature to read the NTC (Negative Temperature Coefficient) thermistor information of the pixel modules. The pixel modules have two types of NTC thermistor positions as described below [7].

- NTC thermistor type 1 - For this type, there are 17 positions to solder a NTC thermistor, as shown in Fig. 3.5 [8]. These NTC thermistor pads are also connected in parallel and distributed around the pixel module, making it possible to measure temperatures just above the ASIC chips. Also, due to the parallel connection, if two or more NTC thermistors are loaded on these positions, it is possible to read the average of these. This was the NTC thermistor which is explained in the introduction to this section.

- NTC thermistor type 2 - There is only one place for the NTC thermistor of this type, and is routed to two pads near the edge of the detector. This NTC thermistor is referred to as the Interlock NTC. This is because it will be used by the interlock system to independently monitor the temperature of the pixel modules, and give feedback to the QA-QC testing system in case of an emergency[9]. This point is to be

[7]The NTC thermistors used for the pixel modules are TDK NTCG series, with 10 kΩ resistance at 25°C.

[8]This image was taken by Shohei Shirabe of Tokyo Tech. during the pixel module production in the summer of 2020.

[9]For example, if the cooling system shuts down accidentally, the temperature of the pixel modules will

soldered by wires, and the other end of the wires are to be soldered to the power adapter card interlock NTC pads which are shown in Fig. 3.3.

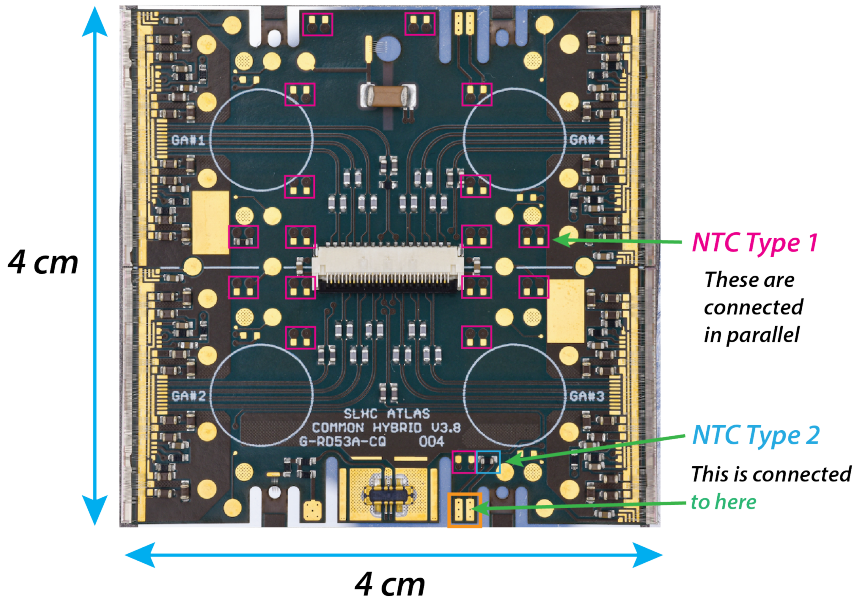


Figure 3.5: The location of the NTC thermistors on the Quad Module.

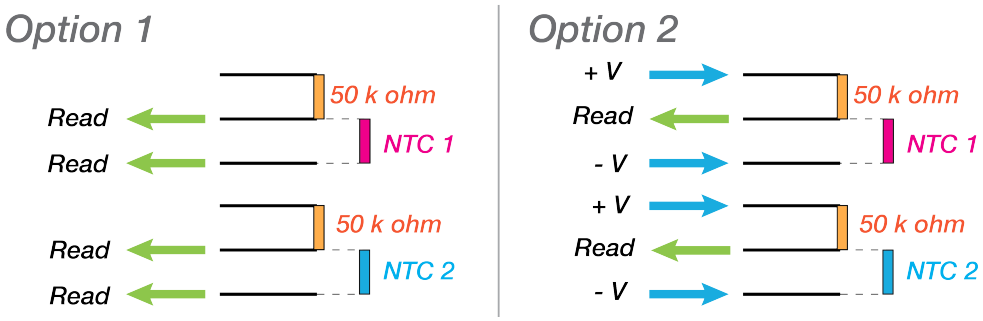


Figure 3.6: The two options to read the NTC thermistor values from the power adapter card NTC block pin headers. Option 1 - Read them directly. Option 2 - Form a potential divider with the 50 kΩ resistors, and read the voltage in the middle of the divider.

increase suddenly. Hence, the interlock system will detect this through the interlock NTC, and shut down the power supplies.

To read the temperature information of the two NTC types, the power adapter card has three dedicated pins for each type (six pins in total). The purpose of this is to use these three pins as a potential divider with the 50 kΩ resistors on the back of the power adapter card. However, the NTC thermistors can also directly be read from these pin headers, as shown in Fig. 3.6.

If the potential divider option is chosen, then a known voltage difference should be applied to the two pins on the corner, and the voltage at the intersection can be measured.

3.3 Validation tests of the powering chain

After producing the power adapter cards, their performance was validated as follows.

3.3.1 The voltage drop of the powering chain

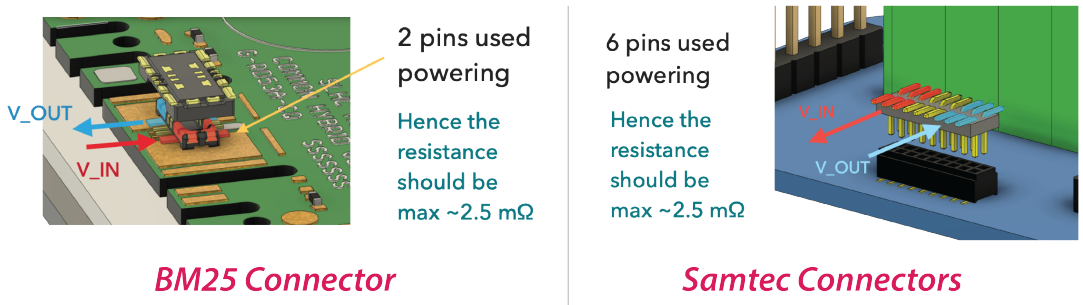


Figure 3.7: The current flows through multiple connectors, which will reduce the effective contact resistance.

The powering chain (from power supply to flex PCB) for the pixel modules were designed to achieve the least voltage drop, as discussed previously in Section 3.1. From Equation 3.2, the resistance of the trace carrying the low voltage power for a maximum rise of 10°C is:

$$R = \frac{0.0171 \times 0.034}{0.655}(1 + 3.9 \times 10^{-2}) = 0.9\,\mathrm{m\Omega}\,,$$

which is negligible. The maximum contact resistances of Samtec connectors and the BM25 connectors were calculated with the data in Table 3.1. As shown in Fig. 3.7, it was

important to consider the resistance in parallel.

Since 2 pins are used to send current for the BM-25 connectors, the max resistance is $2.5\,\Omega$. For the Samtec connectors, 6 pins are used to carry power. Hence the max resistance is $2.5\ \Omega$, the same as the BM-25 connector[10]. With the above information, all resistances except for the power-pigtail were estimated as shown in Fig. 3.8.

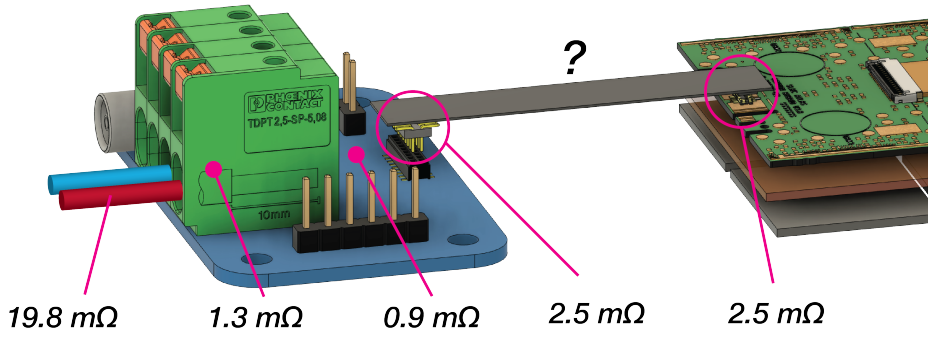


Figure 3.8: The different resistances of the powering chain.

The total resistance of the powering chain is:

$$R_{total} = 19.8\ \mathrm{m}\ \Omega + 1.3\ \mathrm{m}\ \Omega + 0.9\ \mathrm{m}\ \Omega + 2.5\ \mathrm{m}\ \Omega + \mathrm{R}_{\text{power pigtail}} + 2.5\ \mathrm{m}\ \Omega$$
$$= 27\ \mathrm{m}\ \Omega + \mathrm{R}_{\text{power pigtail}}\ . \quad (3.4)$$

At 4.4 A of current, the voltage at the power supplies was 1.962 V, and the voltage on the flexible PCB was 1.51 V. Hence, 0.452 V (at 4.4 A) voltage drop was observed from the power supply to the flexible PCB.

From Equation 3.4, the resistance of the power pigtail was calculated as:

$$R_{powerpigtail} = \frac{0.452\ \mathrm{V}}{4.4\ \mathrm{A}} \times \frac{1}{2} - 27\ \mathrm{m}\Omega = \sim 27\ \mathrm{m}\Omega\ ,$$

and hence, the power pigtail contributed to the largest power loss. This was also investigated with thermal images of the powering chain as shown in Fig. 3.9. The power pigtail clearly gets heated up compared to the other components in the powering chain, and reaching 83 °C at 10 A.

[10]It was seen that this was in good agreement with the measured value, as discussed in Section 3.3.2.

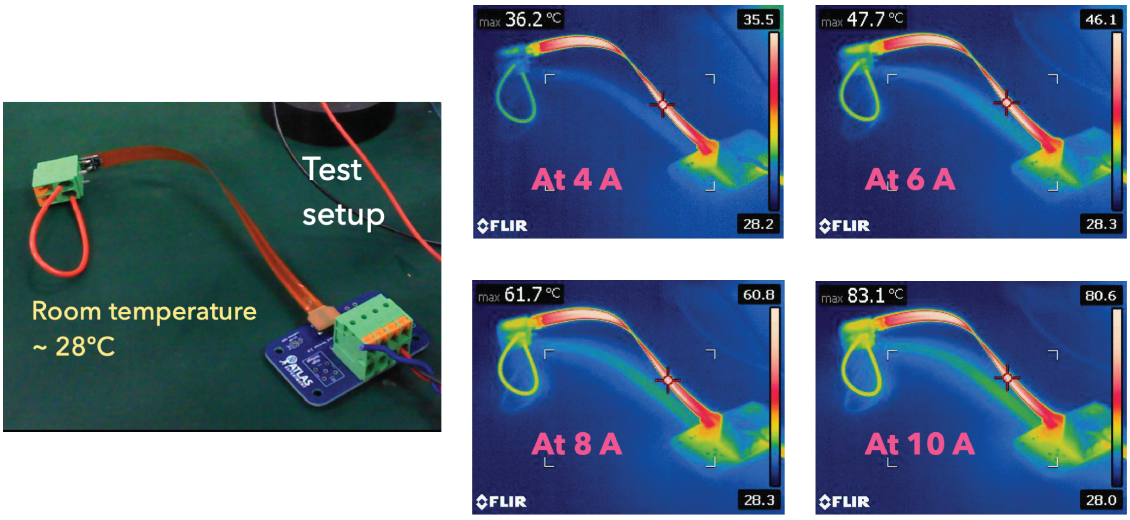


Figure 3.9: The test setup for the temperature measurement of the power pigtail.

After further investigation, it was understood that this increase in resistance was unavoidable for the power pigtail due to the following reasons.

- To make the resistance lower, the copper thickness on the traces need to be increased. However, this is not possible since the power pigtail needed to be flexible, so it can be used as a cable.
- Another way to lower resistance is to increase the width of the traces, as shown in the relation of Equation 3.1. However, due to pixel module cover that the power pigtail has to go through, the width should be less than 8 mm.

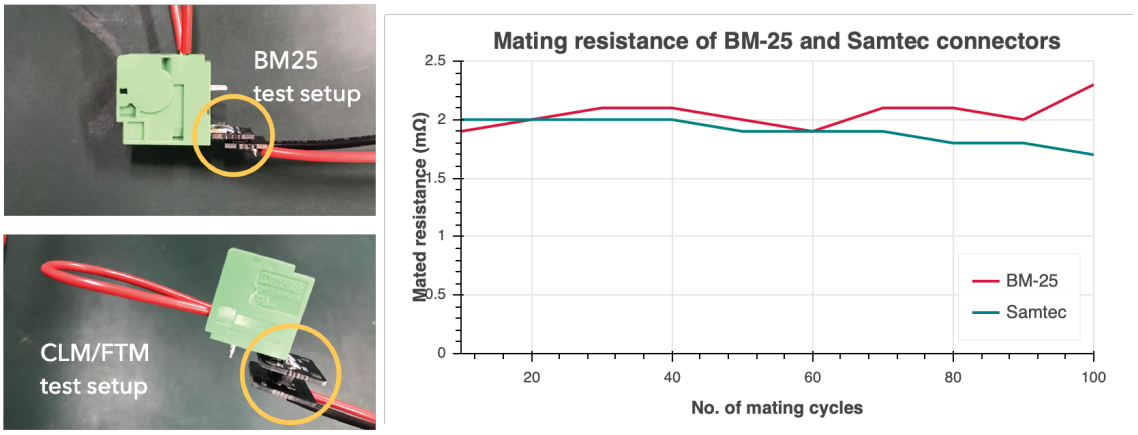
For the next version of the pixel modules, we expect the current to be close to 10 A. Hence, based on the result of this test, we concluded that the next version of the power pigtail will need to be improved to have a wider trace and thicker copper[11].

[11] As mentioned previously, ticker copper will make the cable more rigid. However, the degree of rigidity was not tested, and there is a possibility that a bit more thickness would also be viable.

3.3.2 Power connector mating cycles

Similar to the ZIF connector mentioned in Section 2.3.4, the mating cycles for the power connectors is also important. This is to ensure that contact resistance does not significantly change for several mating cycles, since pixel modules will be attached and detached several times from the powering setup (estimated to be in the order of a 100).

For this test, the contact resistance of the connectors were directly measured with several dedicated PCBs. The setup is shown in Fig. 3.10(a). The part circled in yellow are the two mated connectors, each soldered to a PCB.



(a) (b)

Figure 3.10: a) The setup used for testing the mating cycles of the BM-25 and Samtec connectors. b) The results of the mating cycle test.

The testing procedure is simply measuring the voltage drop at 10 A across two mated points of the connectors, as shown in Fig. 3.10(a). Once the voltage is accurately determined, the resistance value can calculated from Ohms law.

The results are shown in the graph of Fig. 3.10(b). It is understood that there is no significant increase in the contact resistance even after 100 mating cycles, for both connectors. Hence, a large power loss due to mating - unmating will not occur when testing the pixel modules.

3.3.3 High voltage leak current

Due to the silicone glue coating on the CLM pads as shown in Fig. 3.3, it was important to check if there is any significant high voltage leakage current through this glue layer. This was to ensure that there is no influence from leakage current for high voltage measurements. The measured leakage current for the power adapter card with voltage up to 1100 V is shown in Fig. 3.11.

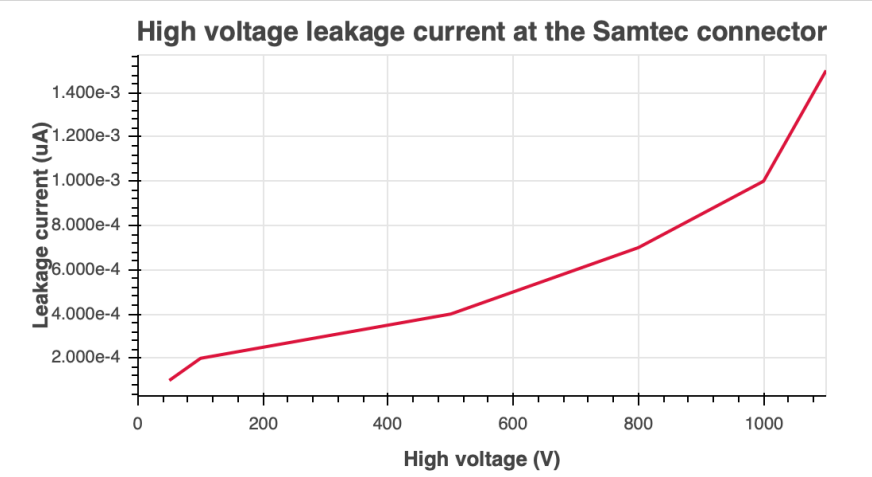


Figure 3.11: The measured leakage current on the power adapter card.

From the voltage vs current measurements for the pixel modules, the minimum current before the breakdown voltage was measured to be greater than 0.1 μA. This is 100 times larger than the largest leakage current seen in Fig. 3.11. Hence, we concluded that there is no issue when supplying HV through the power adapter card.

Chapter 4

Performance evaluation of the DAQ system and pixel detectors

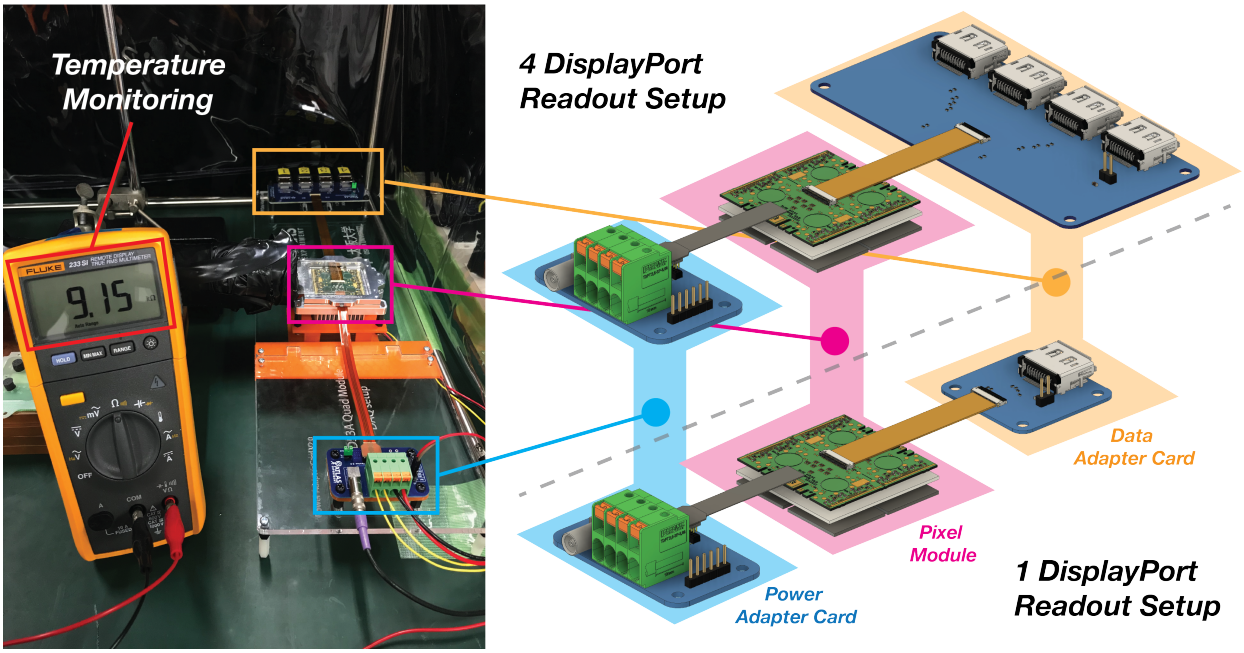


Figure 4.1: The 1-DisplayPort and 4-DisplayPort DAQ setups for pixel detectors. The whole setup is inside a clean-room to avoid any dust depositing on the pixel detectors. The temperature is monitored by measuring the NTC thermistors resistance.

The first pixel modules in the world were produced in Japan in July 2020. After production, the testing system discussed in Section 1.3.3, which includes the adapter

cards discussed in Chapters 2 and 3, was used to verify the performance of the pixel modules. Simultaneously, the performance of the DAQ system was also verified. Figure 4.1 shows the two readout setup options which utilize the developed adapter cards, used for testing the pixel modules.

4.1 Verification of the DAQ system functionality

Using the components mentioned in Chapters 2 and 3, the testing DAQ system was constructed as shown in Fig. 4.1. The downstream DAQ system after the data adapter cards were set up as shown in Fig. 1.10.

The performance of this overall DAQ system is verified by checking the validity of data coming from the ASIC of the pixel detector, at different data rates (160 Mbps and 640 Mbps)[1]. Hence, it was also important to verify the performance of the pixel detectors at the same time.

4.1.1 Verification method of the digital front-end

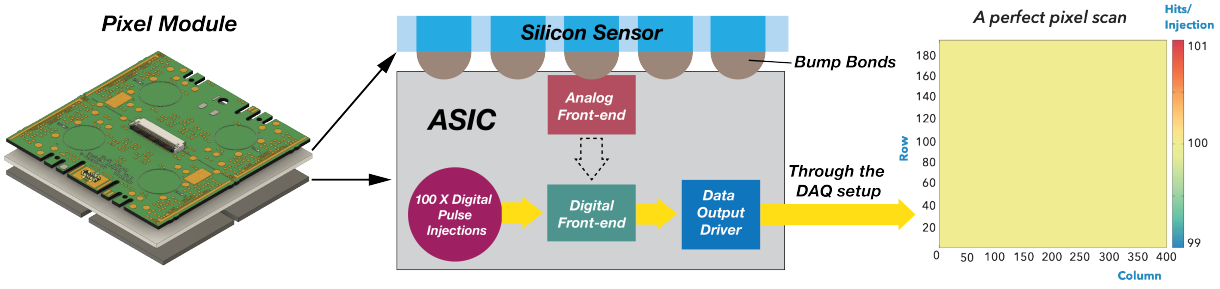


Figure 4.2: Inside the ASIC, the digital front-end digitizes the information coming from the analog-front end. To check the performance of the digital front-end, there is a feature to inject digital pulses. The hit information will be sent at high speeds through the DAQ system to the computer, where it gets plotted as shown in the right.

Each part of the ASIC needs to be verified when evaluating the performance of the pixel detectors. An essential first step of this verification is the correct functioning of the

[1]Data acquisition (DAQ) at 1.28 Gbps is not tested this time, since the firmware (mentioned in Section 1.3.3) for the DAQ framework is still under development.

digital front-end. If it does not function properly, the data coming from the silicon sensor or the analog front-end cannot be verified. For this purpose, the ASIC has a feature to inject digital pulses[2] to the digital front-end. Using this feature, it is possible to check the response of the digital front-ends of each pixel in the pixel matrix. This is known as a **Digital Scan**.

There are $192 \times 400 = 76800$ pixels in one ASIC. A default digital scan has 64 loops[3]. For each loop, first, $76800 \times 63/64 = 75600$ pixels will be deactivated. After then, 100 digital pulses (known as digital injections) will be injected at a 30 kHz frequency (**Trigger Frequency**) to each of the activated 1200 digital front-ends. These 1200 pixels will then be de-activated, and another 1200 will be activated and injected with 100 digital injections. This process is looped 64 times, and results in the whole pixel matrix being injected with 100 digital injections. This digital scan information is sent to the output driver in the ASIC, where it will get serialized at high data rates. The serialized data is then sent over the DAQ setup described in Section 1.3.3, to reach the FPGA receiver at the other end. At the FPGA, one recorded digital injection is considered as one hit, and these hits are plotted in a 2-D histogram called the **Occupancy Map**. For a perfect digital scan, the whole pixel matrix shows 100 hits for each pixel as shown in the right plot of Fig. 4.2.

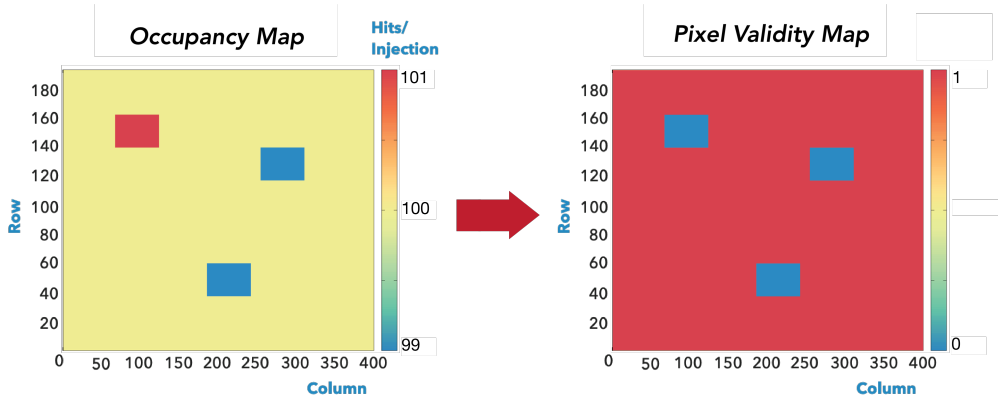


Figure 4.3: A demonstration of obtaining the pixel validity map from an occupancy Map. The pixel blocks which did not return 100 hits are given the value of zero.

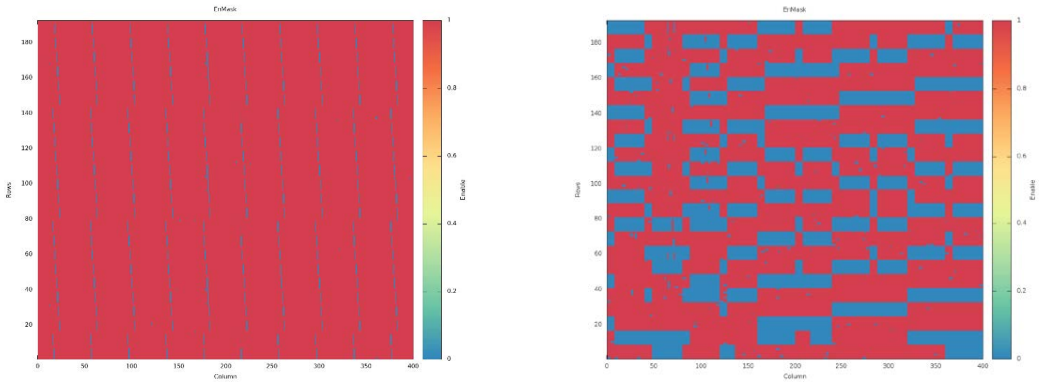
[2]Which pretend as the digital signal after the comparator in the Analog front-end.

[3]The parameters like number of injections, frequency of injections, and the number of loops can be changed.

Using the *occupancy map*, another plot called the **Pixel Validity Map**[4] is created. Here, pixels which recorded hits for all the injected pulses (100 out of 100) will be given the value of 1. Pixels which did not record hits for all the injected pulses (for example, 101 out of 100, or 98 out of 100) will be given a value of 0. The purpose of this is to identify the pixels which responded strangely, and not to use them for actual operation. A demonstration of how the *pixel validity map* is created from an *occupancy map* is shown in Fig. 4.3 (this is not a real example).

4.1.2 Issues with initial DAQ testing

The initial digital scans for the pixel detectors did not return perfect results for the whole pixel matrix. In some cases, the pixel data from some loop stages were not received at the FPGA as shown in Fig. 4.4(a). In more extreme cases, such as the one shown in Fig. 4.4(b) was observed, which is known to be caused when data from a specific data channels[5] were not received at the FPGA.



(**a**) Case 1 (**b**) Case 2

Figure 4.4: The *pixel validity map* of imperfect digital scan results from the initial pixel detector tests. Case 1 - The pattern seen when a loop stage fails in a digital scan. Case 2 - The pattern seen when data from some data channels are not received.

[4]This is a definition used in this thesis to explain this concept in a much simpler way. In the actual DAQ framework, this is known as the EnMask Plot.

[5]Reminder- As explained in the previous Chapters, an ASIC has 4 configurable data channels for transmitting data at high data rates. The 4 DP data adapter card uses only 3 data channels per ASIC, while the 1 DP data adapter card uses 1 data channel.

We considered that these imperfect results were mainly due to the attenuation of serialized signals transmitted from the ASIC data output drivers, which are explained in Section 4.2.1. The next section also discusses how the above issues were fixed by using a software tool which I developed.

4.2 CML Tap Scan

4.2.1 ASIC Data Output Drivers

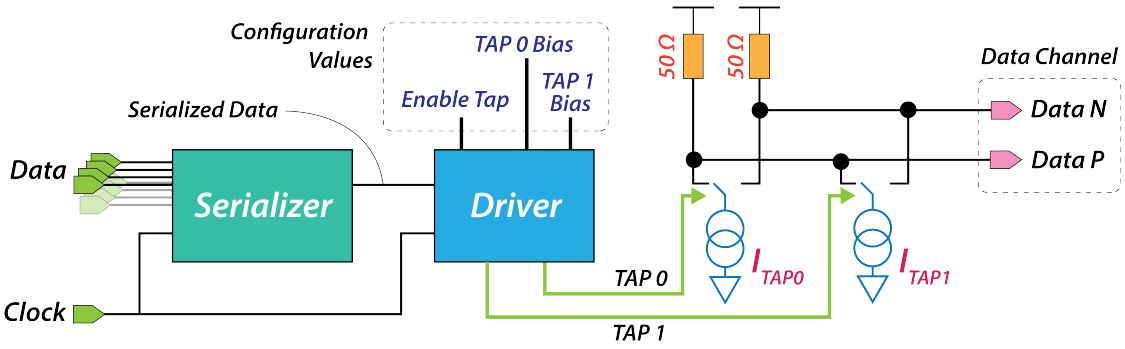


Figure 4.5: The data output drivers of the RD53A ASIC.

There are 4 data output driver blocks (shown in Fig. 4.5) in the ASIC, and one output driver is used for one data channel. This block uses a 640 MHz clock to serialize the encoded[6] output data into differential CML (current mode logic) [11, 30]. This clock can be used to serialize the data up to 1.28 Gbps, but the speed can be reduced by a factor of 2, 4 or 8. Hence, the possible data transfer rates are 160 Mbps, 320 Mbps, 640 Mbps and 1.28 Gbps.

This output driver also contains a programmable pre-emphasis feature, which helps to compensate for the attenuation of signals in transmission lines. This is explained in detail in the next section.

4.2.2 Pre-Emphasis Feature

When high speed signals propagate through a DAQ system, signal distortion can occur due to several reasons such as attenuation, cross-talk and impedance mismatch [31].

[6]The encoding used in RD53 ASIC chips is Aurora 64b/66b

However, even for a DAQ system where the impedance matching is perfect and cross-talk effects are significantly reduced, attenuation effects can still occur [32].

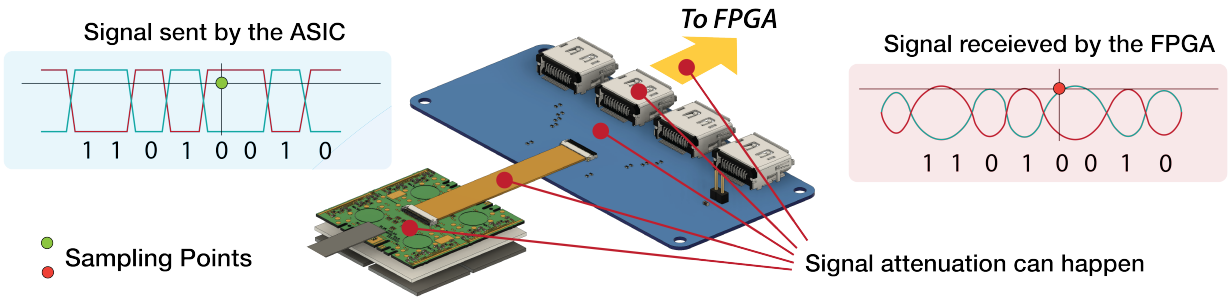


Figure 4.6: The signals from the ASIC will distort when travelling downstream due to attenuation at the points shown in red and yellow.

For the DAQ setup used for testing pixel modules shown in Fig. 4.6, the signal attenuation can occur through the whole signal transmission setup. Due to this attenuation, the signal will get distorted, and the BER (bit error ratio) will increase at the sampling points shown in Fig. 4.6.

The ASIC has a feature called **pre-emphasis**, where it is possible to add a programmable overshoot to increase the high frequency component. This overshoot is added to the first bit of a consecutive stream of bits with the same state, as shown in Fig. 4.7.

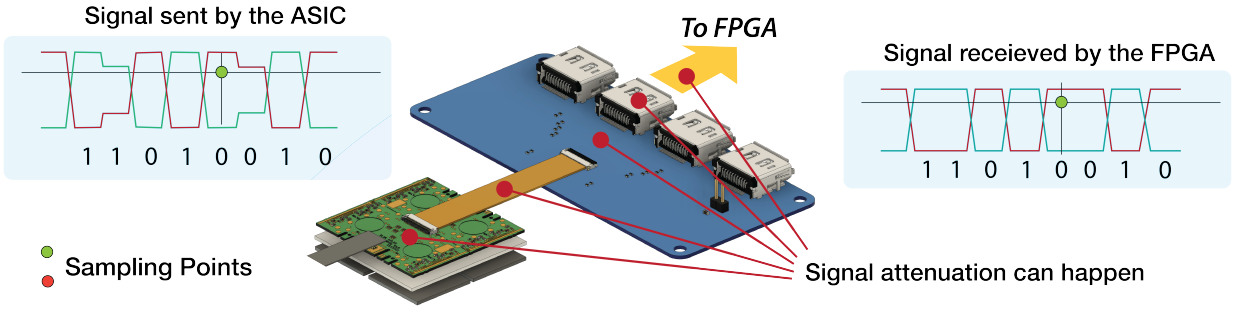


Figure 4.7: By adding pre-emphasis to the serialized signals, a near to perfect signal can be obtained at the FPGA.

The high frequency components attenuates when travelling through the DAQ system, and

with a sufficient pre-emphasis, the originally intended signal can be retrieved at the FPGA.

The ASIC has 2 current mode switches (known as **CML Taps**) in parallel as shown in Fig. 4.5. By changing the values of these switches, one can control the current passing through the output stage current sources. This feature can increase the swing of the signals, and add pre-emphasis to the output signal.

The Tap 0 is always enabled, and Tap 1 can be enabled or disabled using a 1-bit register. Each Tap also has a 10-bit register (known as Tap Bias) [30] which can configure the amount of current flowing through the output stage current sources[7]. Table 4.1 shows these register values and how they need to be changed to achieve pre-emphasis.

Feature	Enable Tap	Tap 0 Bias	Tap 1 Bias
Swing only	0	$1 \sim 1024$ (Default 600)	0
Pre-emphasis	1	$1 \sim 1024$ (Default 600)	$1 \sim 1024$

Table 4.1: The configuration settings for the CML taps of the ASIC data output drivers.

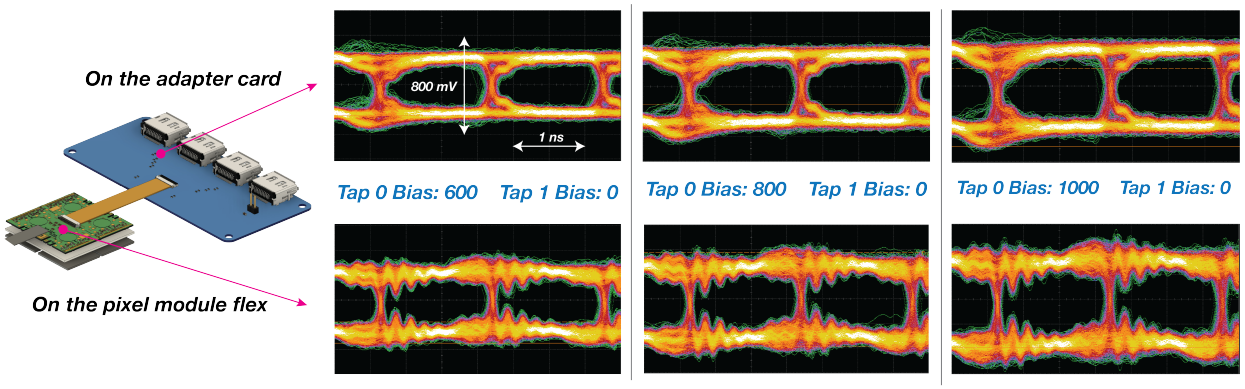


Figure 4.8: A pile-up of 640 MHz serialized signals. The shape of the eye corresponds to 1 bit. By increasing the Tap Bias 0, the swing of the serialized signals can be increased.

Increasing only the Tap 0 Bias (without enabling the Tap 1) only increases the swing of the signals, with no pre-emphasis. Figure 4.8 shows the measured oscilloscope[8] signals on the flexible PCB (near the ASIC) and on the data adapter card, when Tap 0 Bias is

[7] Each increase in bit will correspond to increasing approximately 14 μA.
[8] Using an Agilent 4 GHz Oscilloscope - Infiniium 9000 series, with active differential probe.

increased. Since this oscilloscope image is a pile up of signals, each eye represents 1 bit. It is clearly seen from this figure that the swing of the signals are increased. The oscillation seen on the signal at the flexible PCB is not yet clearly understood, and requires a further study in the future. However, it is possibly caused by oscillations in the ASIC output driver.

When Tap 1 is enabled, and Tap 1 Bias is increased, it adds pre-emphasis to the serialized signals. Figure 4.9 shows the measured oscilloscope signals when Tap 1 Bias is increased.

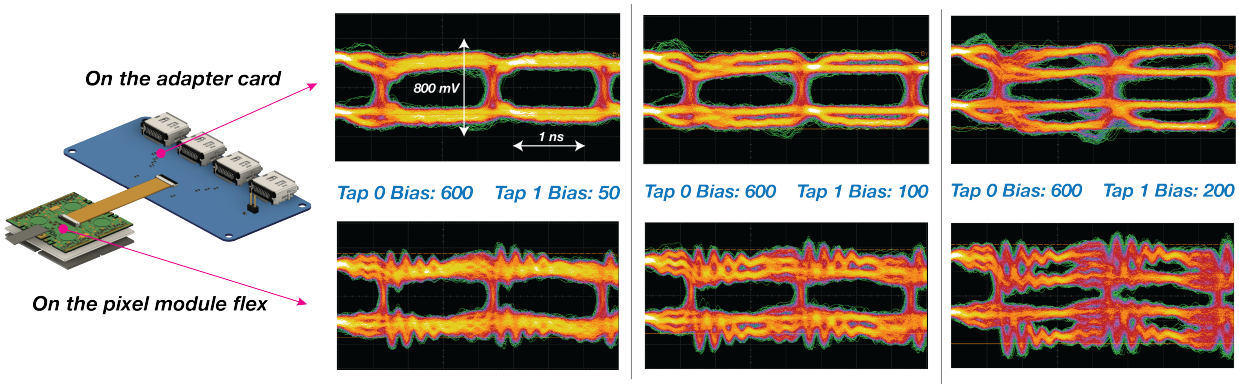


Figure 4.9: A pile-up of 640 MHz serialized signals, and the shape of the eye corresponds to 1 bit. By increasing the Tap Bias 1, pre-emphasis is added to the serialized signals.

It is clearly seen from Fig. 4.9 that increasing the Tap 1 Bias will increase the difference in amplitudes between the piled-up signals[9], and increase the pre-emphasis. This overshoot in the signal sent from the ASIC gradually attenuates as it reaches the adapter card. However, the FPGA receiver is further downstream and the serialized signals are expected to attenuate even more. For small Tap 1 Bias values, this meant that the signals were distorted even more when reaching the FPGA. Hence, signals were expected to have a relatively large pre-emphasis to preserve the signal integrity when reaching the FPGA.

[9]The bits with the high frequency component added, and bits with this component not added are seen piled-up in the region for 1 bit. The difference in the two top (or bottom) lines is the amplitude of pre-emphasis.

4.2.3 Scanning by changing the pre-emphasis

By changing the CML taps, digital scans were performed to check if the increase in signal integrity helps to reduce the number of imperfect pixels. For this, a software tool called the **CML Tap Scan** was developed. The flowchart for the CML tap scan is shown in Fig. 4.10. It first sets a Tap 0 Bias value[10] between 600-1000, and a Tap 1 Bias value[11] between 0-700. The Tap 0 Bias values are increased in a step size of 100, and Tap 1 Bias values are increased in a step size of 50 [12]. Then it will run steps 1 - 3 in a loop.

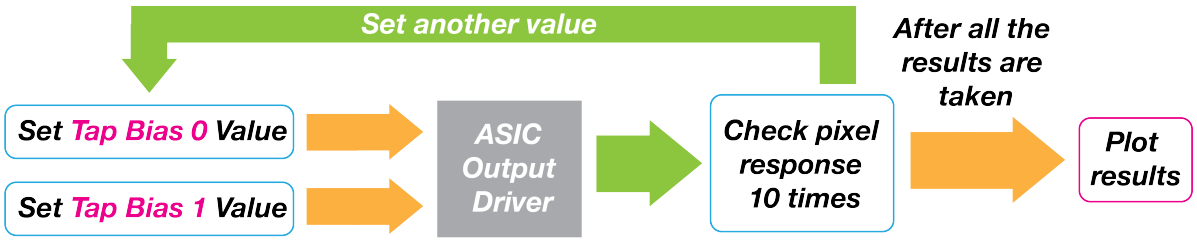


Figure 4.10: The flow of the Tap Scan tool.

- Step 1 - Configure the ASIC using the chosen set of Tap Bias values.
- Step 2 - Send 100 digital injections to each pixel, and verify if these 100 injections are recorded as hits at the FPGA.
- Step 3 - If 100 hits are not registered, then this pixel is defined as a **failing pixel** for the digital scan. The number of failing pixels are counted for the whole pixel matrix.

After steps 1-3 are done, the average of the number of failing pixels are taken. The average is taken to avoid failing pixels appearing randomly, for a certain tap value [13]. After all the average numbers of failing pixels for each Tap Bias set is obtained, this data-set is used to plot the results.

[10] Since 600 is the default value, it was chosen to increase from this default value. 1000 is set as the upper limit since the register is 10-bit.

[11] 700 is set as the upper limit, because the jitter will even more beyond this, as explained later.

[12] These step sizes were chosen because the results don't change significantly between these steps, and large steps meant less time for the scan.

[13] If failing pixels appear 2 out of 10 times, then there is a 80% probability the Tap Bias values for this region is considered as stable for 1 scan. However, this region is not completely stable, and these regions should be avoided when deciding the most stable Tap Bias values.

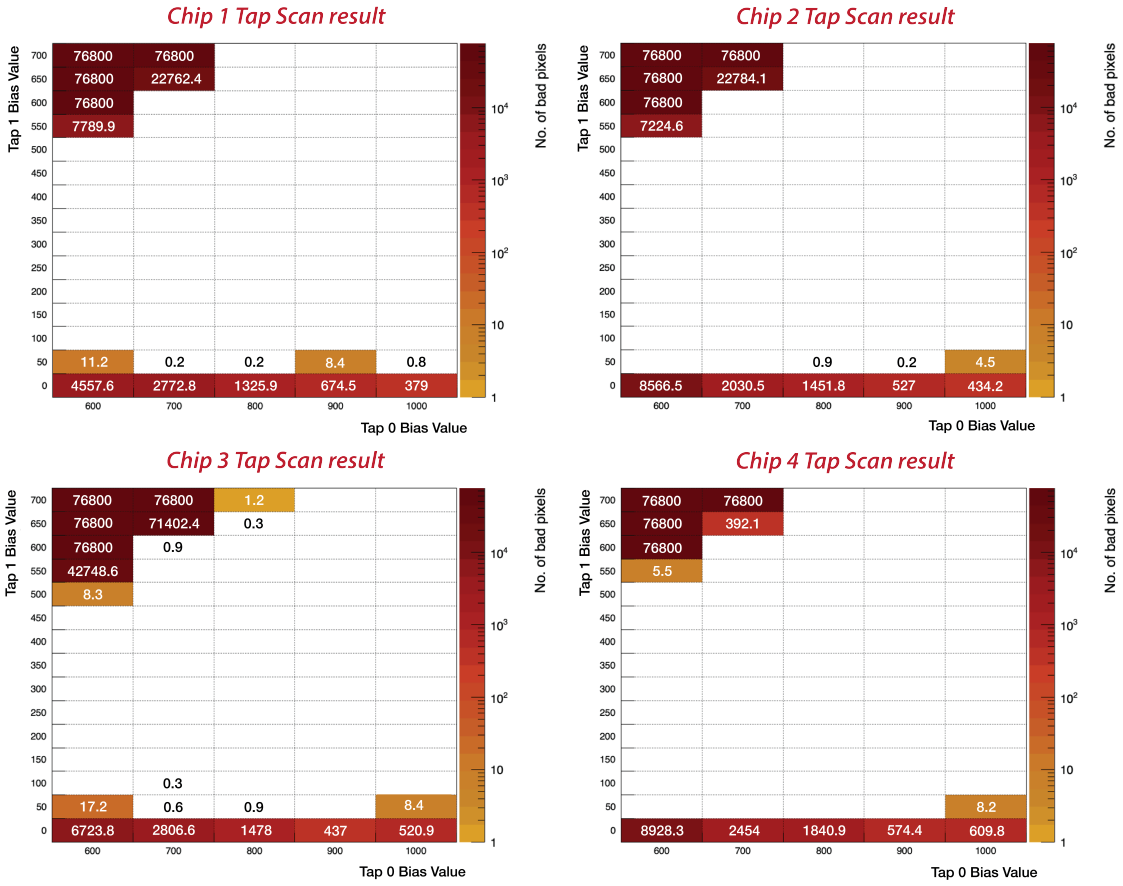


Figure 4.11: The Tap Scan result for different ASIC chips in the pixel module. The speed of the DAQ is 640 Mbps.

The scan results that were obtained using this Tap Scan tool for Chip 1 to Chip 4 of the pixel module are shown in Fig. 4.11. The X and Y axis of these plots are Tap 0 bias and Tap 1 bias values, respectively. The Z axis (in log) is the number of failing pixels, which is also shown inside each box for that particular CML Tap bias value. If the box is empty, it means that the number of failing pixels are zero.

The observations stated below were made for all 4 ASIC chips in the pixel module.

- Observation 1- For the default configuration values (Tap 0 Bias- 600, Tap 1 Bias- 0), the number of failing pixels are high.
- Observation 2- Just increasing the swing of the signals (through Tap 0 Bias) does not

decrease the number of failing pixels significantly.

- Observation 3- Adding pre-emphasis (through Tap 1 Bias) was more effective in reducing the number of failing pixels.
- Observation 4- Excessive pre-emphasis will increase the number of failing pixels.

Observation 1 shows that the default tap bias values of the ASIC, which were recommended based on circuit simulations [30], was not the best configuration for the pixel module. Hence, a new default configuration value needs to be set.

The signal which enter the MMA Ohio card will go through a buffer, before reaching the FPGA. Due to this, even if the swing is increased, the shape of the signal will stay the same. Hence, the contribution of increasing just the swing is not sufficient to compensate for the attenuation of signals. This is what the observation 2 shows.

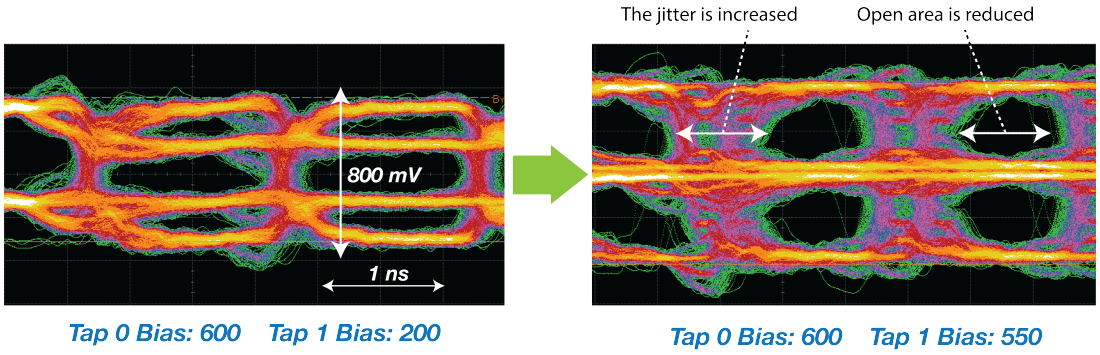


Figure 4.12: Increasing the pre-emphasis too much will increase the signal jitter, and this will reduce the open area.

Hence, as stated in observation 3, pre-emphasis was necessary to compensate for the attenuation of signals on the data lines. However, increasing the tap 1 bias too much will transfer some of pre-emphasis to the next bit as shown in Fig. 4.12, and the reduction of the open area will now create more bit errors. This is stated in observation 4.

Hence, the new configuration of tap bias values for the quad pixel detector was determined as **Tap 0 Bias: 600** and **Tap 1 Bias: 200**. With these new configuration values, several digital scans at 640 Mbps were done for all the chips. The results are shown in Table 4.2.

ASIC Chip	No. of Scans	Result	Obtained BER upper limit
Chip 1	2980 scans	Zero failing pixels	1.6×10^{-12}
Chip 2	1470 scans	Zero failing pixels	3.3×10^{-12}
Chip 3	1570 scans	Zero failing pixels	3.0×10^{-12}
Chip 4	1470 scans	Zero failing pixels	3.3×10^{-12}

Table 4.2: The result of multiple digital scans for the new tap bias values. The speed of data transmission is 640 Mbps.

The BER upper limit for the measurements is calculated using Equation 4.1, which is similar to Equation 2.4.

$$BER_{\,measured\ upper\ limit} = \frac{3\ \text{biterrors}}{\text{No. of scans}} \times \frac{1}{76800\ (\text{No. of pixels per ASIC})} \times \frac{1}{10\ (\text{No. of loops})} \times \frac{1}{100\ (\text{No. of digital injections})} \times \frac{8(\text{Number of pixels per data frame})}{66(\text{Data frame size})}. \tag{4.1}$$

The results for measured BER upper limit, shown in Table 4.2 is significantly low. However, the calculation result of the required BER upper limit in Section 2.3.2 was 9.5×10^{-13}, and the measured result has the same order of magnitude as the required upper limit. We consider that the developed DAQ system (including the DAQ frameworks mentioned in Section 1.3.3) can be used in QA-QC of pixel modules, but another order or two magnitude of data is required to confirm this.

4.3 Voltage Trim Scan

The power to the ASIC is supplied through a Shunt + Low Dropout (SLDO) regulator which is explained in Section 4.3.1. The performance of the SLDO regulator has been tested previously for a single ASIC chip, but a 4-chip operation could not been conducted till the quad pixel modules were produced.

In a pixel module, since the 4 ASIC chips share current (as explained in Section 3.2), there was also concern if the shared current will cause problems for operating the ASIC chips[14]. On top of this, each ASIC chip will have a slight difference in voltage values it regulates, and it was necessary to see if these differences between ASIC can affect the performance of the pixel module.

To clear these doubts, a software tool called the voltage trim scan was developed when testing the first pixel modules in Japan, and it is explained below in this Section.

4.3.1 The SLDO Regulator

The ASIC core is powered by two internal voltage rails, analog voltage (VDDA) and digital voltage (VDDD). The supplied voltage at constant 4.4 A current is regulated to the 2 voltages by two Shunt + Low Dropout (SLDO) regulators. The control circuit in the SLDO regulator ensures that the external power supply pads sink a constant current independent of the ASICs internal current consumption, and generate a regulated internal voltage [11].

The SLDO regulator output voltages, VDDA and VDDD, are regulated by two configuration values of a 5-bit register known as **analog trim** and **digital trim**. When a pixel module is powered, the SLDO regulators will power the ASIC core with default VDDA/VDDD corresponding to analog trim = 16, and digital trim = 16. If the chip core is properly powered and is able to receive the CMD + CLK signal coming from the FPGA (referred as configuring), then the analog trim and digital trim values can be changed to set the analog voltages and digital voltages supplied to the ASIC chip core.

[14] If one ASIC consumes a lot of current, the other ASIC chips will not get enough current.

4.3.2 Verification of the SLDO

First, it was important to verify if the VDDA/VDDD at analog trim = 16 and digital trim = 16 values are high enough to power the ASIC core properly. Since each SLDO has a small individual behavior when regulating voltage, some ASIC chips are not configured for the default VDDA and VDDD. As a solution for this, the pixel module has an option to pull-up SLDO output voltage by a few volts [15].

Table 4.3 shows the measured VDDA and VDDD for different analog and digital trims, for the first pixel module tested in Japan. It also shows how the VDDA at analog trim = 16 is changed due to the addition of a pull-up resistor.

ASIC Chip	Voltage	Trims (16,16) before pull-up	Pulled-up resistor	Trims (16,16) after pull-up	Trims (22,22) after pull-up
Chip 1	VDDA	1.067 V	150 kΩ	1.162 V	1.217 V
	VDDD	1.212 V	-	1.213 V	1.264 V
Chip 2	VDDA	1.120 V	300 kΩ	1.159 V	1.225 V
	VDDD	1.147 V	-	1.147 V	1.193 V
Chip 3	VDDA	1.127 V	300 kΩ	1.174 V	1.234 V
	VDDD	1.135 V	-	1.135 V	1.183 V
Chip 4	VDDA	1.139 V	None	1.139 V	1.201 V
	VDDD	1.135 V	-	1.135 V	1.184 V

Table 4.3: The SLDO output voltage values at different trim values, before and after adding pull-up resistors. For trims, it is represented as (analog trim, digital trim). Note that VDDA cannot be pulled up.

After the configuration is verified, the second verification is to check if the ASIC core works as expected for different output voltages of the SLDO regulator. As explained previously, the output voltages can be changed by modifying the analog and digital trim values. Moreover, since current will be shared between all 4 ASIC chips in a pixel

[15] This is done by adding a pull-up resistor between the output and the reference voltage of the SLDO regulator. A 300 kΩ pull up resistor will pull-up the SLDO output voltage by 0.005 V, and a 150 kΩ resistor will pull-up the voltage by 0.01 V

module, it was also important to check if current consumption by ASIC core in one chip affects the performance of the others.

4.3.3 Scanning by changing the SLDO trims

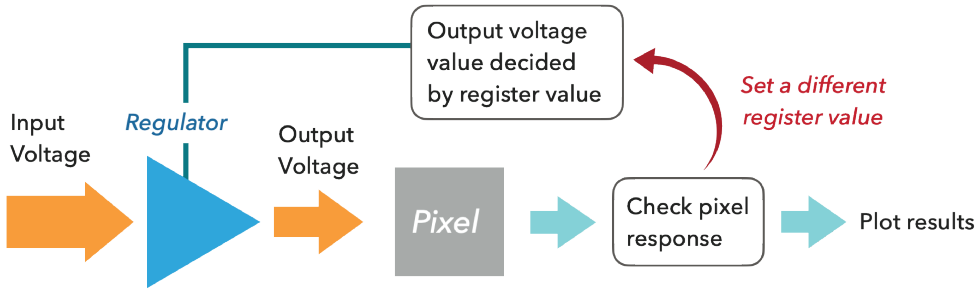


Figure 4.13: The flowchart of the Trim Scan software

For the verification of the SLDO regulators mentioned in the previous section, a software tool called the Trim scan was developed. The flowchart of the software is shown in Fig. 4.13, and it uses a similar approach as the CML tap scan. It first sets an Analog Trim value[16] between 10-26, and a Digital Trim value between 10-26. Then it loops the steps 1 to 3 below, each time setting a new pair of trim values.

- Step 1 - Configure the ASIC using the chosen set of Trim values.
- Step 2 - Send 100 digital injections to each pixel, and verify if these 100 injections are recorded as hits at the FPGA.
- Step 3 - If 100 hits are not registered, then this pixel is defined as a **failing pixel** for the digital scan. The number of failing pixels are counted for the whole pixel matrix.

After the number of failing pixels for each Analog Trim and Digital Trim sets are obtained, this data-set is used to plot the results. These tests were conducted after verifying the stable operation of the pixel modules through the CML tap scan, so there is no bias to the trim scan results.

[16]Since the trim values are 5 bit registers, it can be raised till 32. However, if it's raised beyond 1.3 V, then it will damage the ASIC. This upper limit is roughly around 26, as seen from the measured results in Table 4.3.

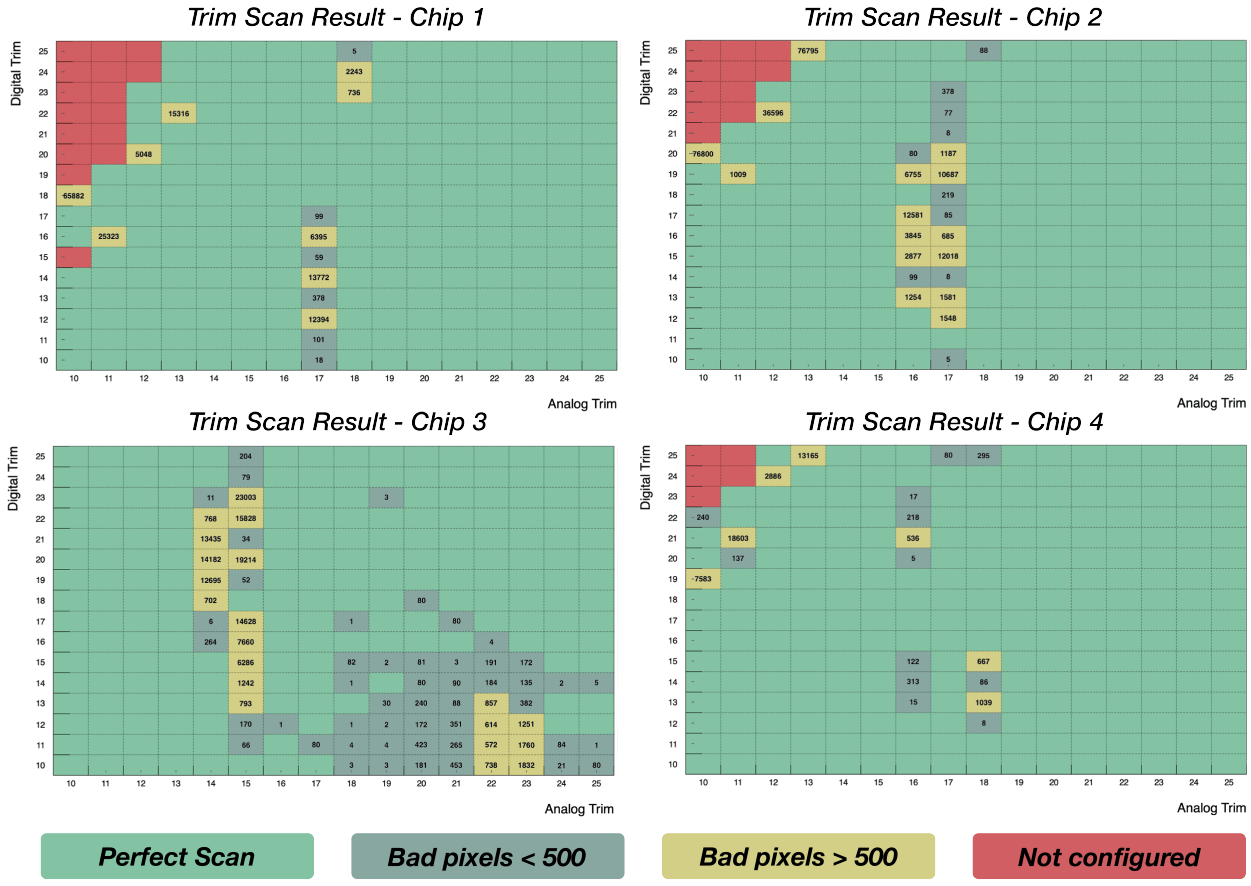


Figure 4.14: The variation of trims for different chips in the pixel detector. The green-yellow regions are defined for when ASIC chips are configured, and the red region is defined for when ASIC chips are not configured.

The plots obtained for the trim scan of all 4 chips are shown in Fig. 4.14. Here, light green regions are where there are zero failing pixels recorded. Perfect digital scans are obtained for trim value sets in those regions. The dark green regions and the yellow regions show that there are failing pixels, but the pixel module is still configured. The red region shows that the pixel module could not be configured. The number of the failing pixels are also shown in each slot for the trim pairs.

These plots show that there is a wide range of trim values where the pixel module can be operated without giving failing pixels. However, some difference due to the individual behavior of each SLDO regulator is observed. For trim pairs, there is a band which give

failing pixels, and the size of this band varies between ASIC chips. The reason for this band is not clearly understood, and will be studied in the future.

Even with these differences, at the usual choice for the operating region for the ASIC, which is around trim values (22, 22), digital scans gave zero failing pixels. Hence, through this test, we confirmed that the SLDO regulator can be properly operated in a 4 chip operation as well.

4.4 Optimization of the DAQ system

After the stable operation of the DAQ system was verified as discussed in Section 4.2, optimization of the DAQ for pixel module testing was considered.

During mass production and QA-QC, several pixel modules (2000 in Japan) need to be tested through different QA-QC procedures. As discussed in Section 1.3.2, one of this procedures is the verification of the 4 ASIC chips in the pixel module. If a long time is taken for this stage, the other QA-QC procedures will be delayed. Hence, reducing the time for testing the ASIC performance is important.

4.4.1 The speed of data transfer

For making the evaluation process of the ASIC faster, the trigger frequency for scans can be increased. However, due to the instability described in Section 4.1.2, the upper limit of the trigger frequency for digital scans described in Section 4.1 could not be determined accurately.

The average time (of 10 scans) taken for a digital scan vs the trigger frequency of digital scans, and the number of failing pixels[17] vs the trigger frequency are shown in Fig. 4.15. The plotted results are for four different scenarios mentioned below.

- A digital scan for 1 ASIC chip, when data is received at the FPGA through 3 data channels.
- A digital scan for all ASIC chips, when data is received at the FPGA through 3 data channels.
- A digital scan for 1 ASIC chip, when data is received at the FPGA only through 1 data channel[18].
- A digital scan for all ASIC chips, when data is received at the FPGA only through 1 data channel.

For all the tests, the 4-DisplayPort data adapter card was used, but reading out through one data channel is similar to the case of using the 1-DisplayPort data adapter card.

[17]The failing pixels here have the same definition with the ones in the CML Tap Scan and Voltage Trim Scan.

[18]Reminder- The data channels in the ASIC can be enabled and disabled.

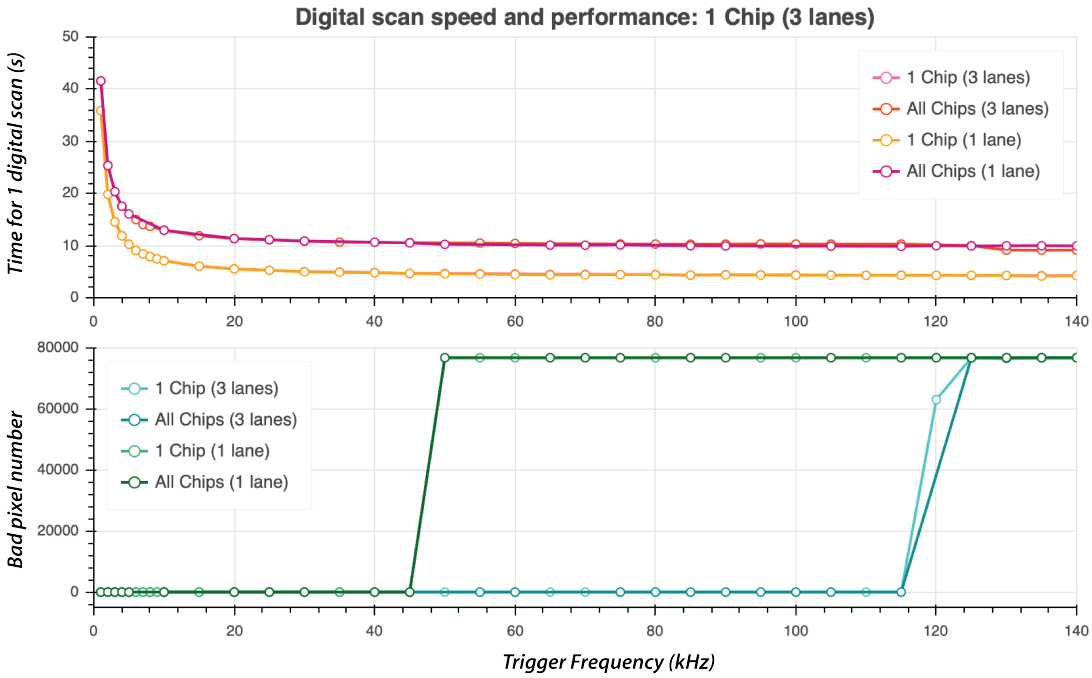


Figure 4.15: The time taken for digital scans and the variation of the number of failing pixels with trigger frequency of digital scans. In the top plot, the 1 Chip scenarios and all chip scenarios have overlapped, making it hard to see the difference. In the bottom plot, 1 lane scenarios and 3 lane scenarios have overlapped.

As shown in Fig. 4.15, it is possible to increase the trigger frequency of digital scans well beyond the default value of 30 kHz for a 3-data-channel readout. Once it crosses the 115 kHz point, bottlenecks in the FPGA processes will cause data corruption and increase the number of failing pixels. However, the time taken for digital scans does not change much beyond 40 kHz due to the finite time taken for software processes to complete. When all four chips are operated simultaneously, this finite time is larger, as seen by the vertical shift in the top two graphs of Fig. 4.15. This was expected, since the amount of data needed to be processed by the software is more, and it will take more time to complete the digital scan.

The situation for the time taken for digital scans when data is readout from just one data channel is similar to the 3-data-channel case discussed above. However, as shown in Fig. 4.15, the number of failing pixels will increase beyond the 45 kHz point.

Through these results, we determined that the trigger rate for scans can be optimized at 40 kHz, since beyond 40 kHz the scan time did not reduce significantly. Further, at 40 kHz trigger frequency, the digital scans return perfect results regardless of the number of data channels used for reading out data from an ASIC chip.

Chapter 5

Conclusion

The DAQ system which is used for the quality assurance and quality control of pixel modules during mass production needs to be developed in stages. This system was first developed for testing the prototype pixel modules, and it will be improved in the coming years to the final DAQ system used during mass production.

For this DAQ system used for testing prototype pixel modules, several interface cards were developed to receive the data coming from the pixel modules, and to supply power to the pixel modules. These interface cards were validated through independent tests, to ensure that their performance was as expected: the measured upper-limit of BER[1] (2.2×10^{-14}) is less than the required upper-limit of BER (9.5×10^{-13}), and the differential impedance is controlled to $100\ \Omega$. The interface cards: the data adapter cards (the 1-DisplayPort version and the 4-DisplayPort version) and the power adapter cards were recognized as the common interface cards to be used by all the testing sites in the world (24 in Europe and 6 in the United States of America). Hence, we produced about 100 of each data adapter card, and 125 of power adapter cards, and shipped to the testing sites in the world. Through this, we managed to make an important contribution to the ATLAS inner tracker upgrade project.

After the testing system was established, it was used to test the first prototype pixel modules produced in the world. We verified that the whole testing system (including the adapter cards) was working well, as validated through the independent tests.

However, when testing the performance of the ASIC chips in the pixel module, there were several pixels in the digital front-end which did not respond perfectly; 100 digital

[1] bit error rate

injections did not return 100 hits for some random pixels. This issue was seen at sites all over the world, when they were testing the prototype pixel modules. After investigating, it was realized that this was possibly due to attenuation of data signals sent from the ASIC transmitter to the FPGA's receiver. The ASIC has a feature to compensate for this attenuation by adding pre-emphasis, but it had not been tested for a pixel module operation. Hence, a software tool (the CML tap scan) was developed to find optimum configuration values for the pre-emphasis feature.

Through this software tool, we managed to solve the issue seen when receiving data from the digital front-end pixels, and achieve a measured upper-limit of BER in the order of 1×10^{-12}; which is roughly equal to the required upper limit. By reporting this result at international meetings, other testing sites in the world also managed to solve these readout issues and establish a stable pixel module testing system.

After a stable operation was established, other features of the pixel module was also evaluated. One was the proper functioning of the SLDO regulators of the ASIC, when all 4 chips in the pixel module were operated at the same time. A software tool (the voltage trim scan) was also developed for this evaluation, and it was established that the SLDO regulators performed without issues in a 4 chip operation as well.

Finally, an evaluation of the speed of testing the pixel modules was also conducted to reduce the time taken for QA-QC procedures. The default trigger frequency for digital scans is set at 30 kHz, and the recommendation was to reduce the trigger frequency of digital scans below 30 kHz when operating using 1 data channel per ASIC. This could not be verified till a stable operation was established through the CML tap scan. After a stable operation was established, the speed could be optimized to 40 kHz; at higher trigger frequencies than previously thought, and independent of the number of data channels used.

Hence, this research achieved the initial objectives and confirmed that the developed DAQ system can be used for testing prototype pixel modules, and a similar DAQ system based on this can be used to assure and control the quality of the final pixel modules at testing sites around the world. Through this, we will succeed in installing pixel modules with reliable performance in the new ATLAS inner tracker system, so that it can be used to search for new physics phenomena at the HL-LHC.

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Appendix A

ATLAS Detector

A.1 The ATLAS inner tracker - after 2013

Figure A.1 shows the orientation of the insertable B-layer (IBL) along the beam pipe.

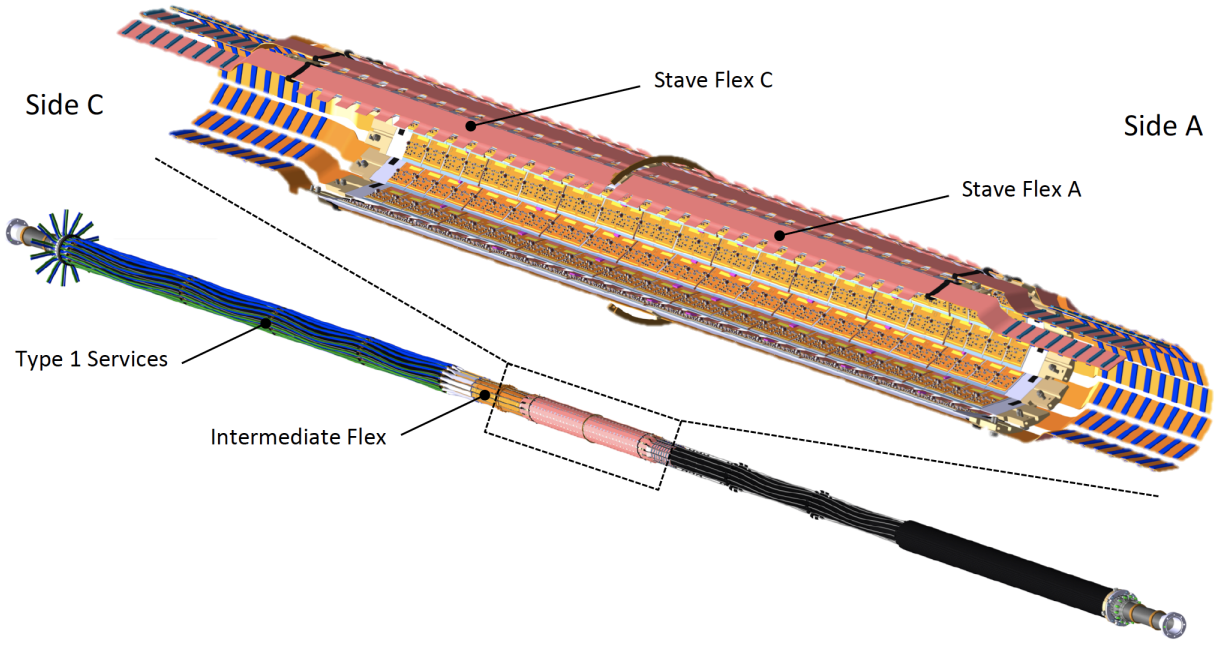


Figure A.1: A 3D view of the IBL, showing its orientation on the beam pipe.

Figure A.2 shows the layout of the ATLAS inner tracker system after the insertable B-layer (IBL) was added in 2013. Both figures are obtained from [4].

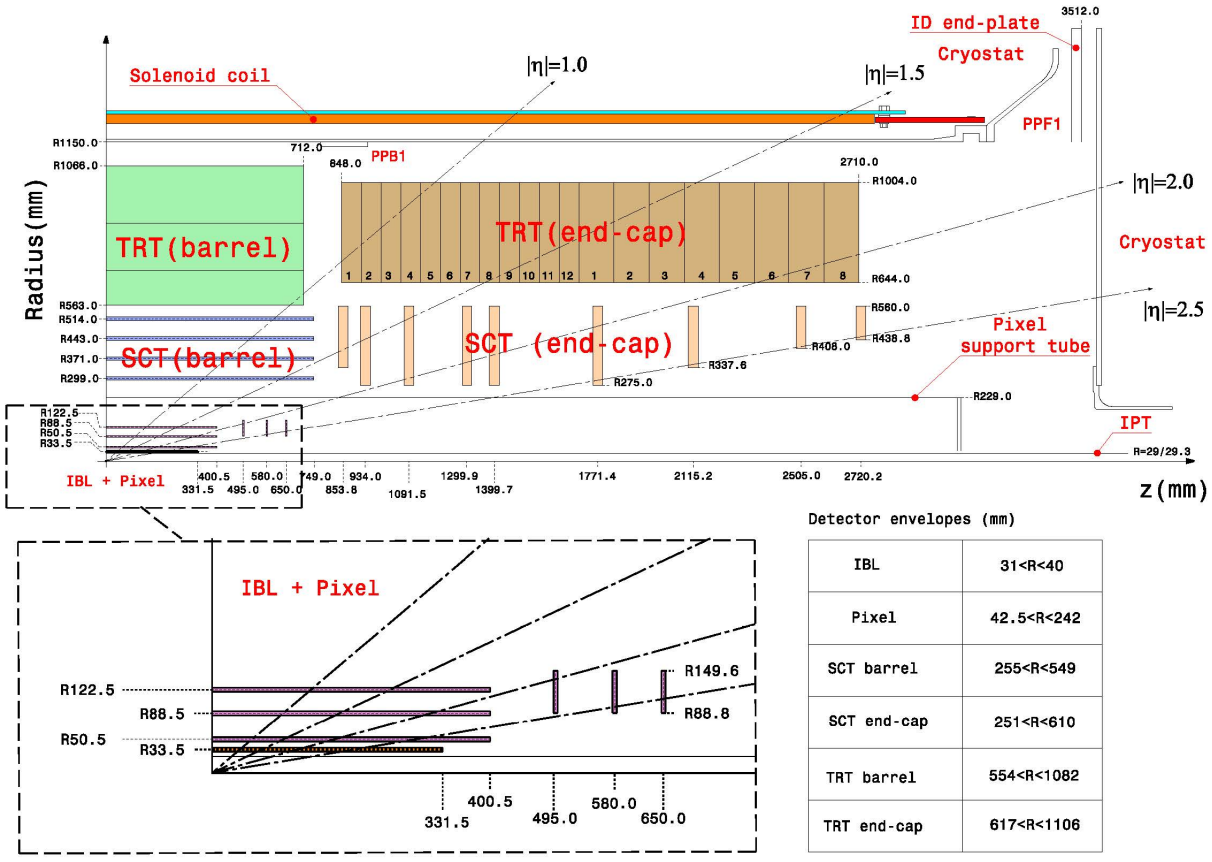
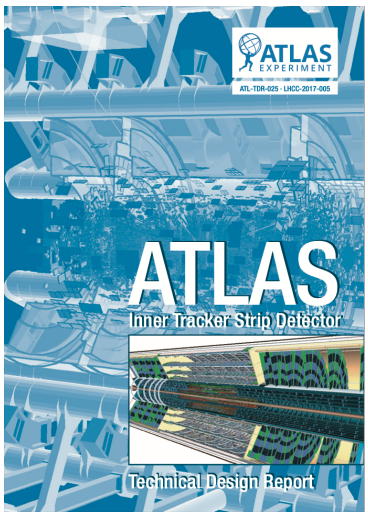


Figure A.2: The layout of the ATLAS inner tracker system, after the IBL was included in 2013.

As mentioned in the Section 1.2.2, this whole inner tracker will be replaced by 2027. The new name given to the inner tracker system is ITk, and will only consist of Strip Detectors (which are similar to semi-conductor trackers (SCT)) and Pixel Detectors.

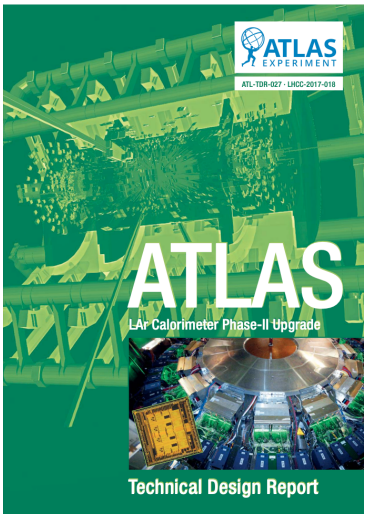
A.2 The technical design reports for HL-LHC

The technical design reports for the HL-LHC upgrade of each sub-detector of ATLAS, shown in Fig. A.3, was approved by CERN in April 2018.

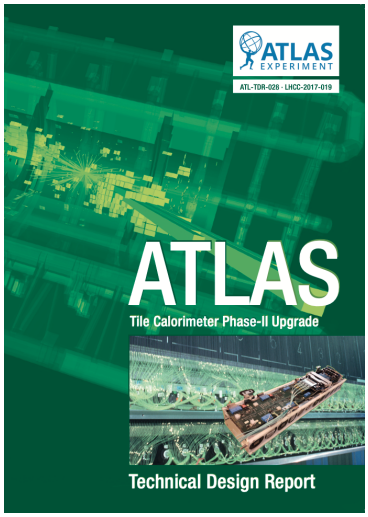


(**a**) Semiconductor Tracker. ATLAS-TDR-025 [33].

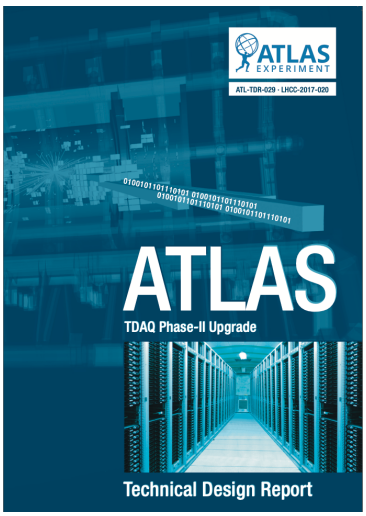
(**b**) Muon spectrometer. ATLAS-TDR-026 [34].



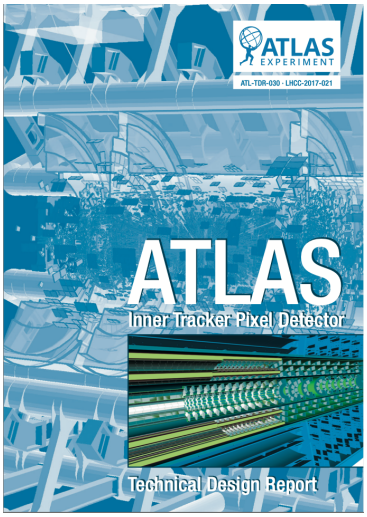
(**c**) Liquid Argon Calorimeter. ATLAS-TDR-027 [35].



(**d**) Tile Calorimeter. ATLAS-TDR-028 [36].



(**e**) TDAQ. ATLAS-TDR-029 [37].



(**f**) Pixel detectors. ATLAS-TDR-030 [10].

Figure A.3: The TDR reports of each subdetector for the HL-LHC upgrade.

Appendix B

Differential Impedance

B.1 Simulation of Differential Impedance

The simulation result which includes the solder mask contribution shows that the differential impedance is controlled to 100 $\Omega \pm 10\%$, for the width of traces being **4 mils** (**101.6** μ**m**), and the space between traces being **6 mils** (**152.4** μ**m**). Hence, these values are taken for traces in the final design.

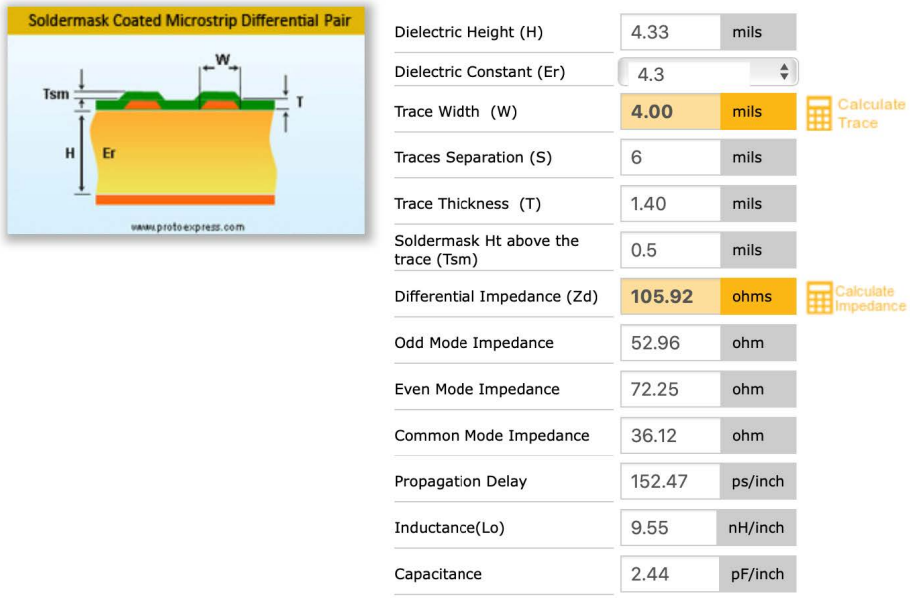


Figure B.1: The simulated trace impedance using Free Impedance Calculator Tool [18].

B.2 Simulation of Via Impedance

The simulated result of the PTH via impedance is shown in Fig. B.2. As mentioned in the text, this is for single ended impedance. However, for differential signals the contribution to impedance from the other via should also be added. This was not used when designing the data adapter cards mentioned in this research, but should be incorporated into future designs.

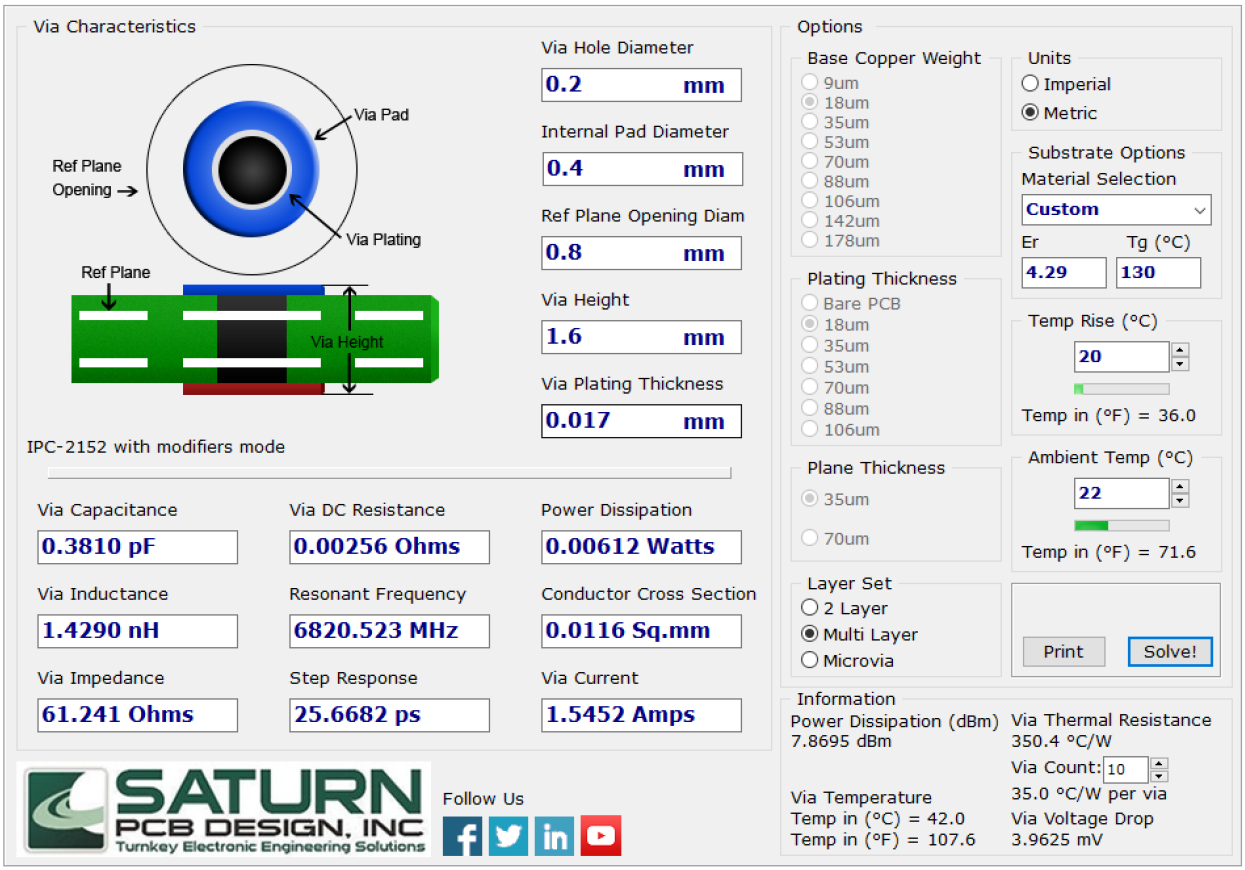


Figure B.2: The simulated via impedance using Saturn PCB Toolkit Version 7.13 [19].

More information on calculating differential impedance of vias can be found at [38].

Appendix C

Cross-talk between signal lines

The cross-talk between signal lines occur when a signal in a conductor couples to adjacent conductor lines, either through capacitive coupling or inductive (or magnetic) coupling. If the adjacent conductors are left floating, capacitive coupling dominates. But even if the conductors are terminated through their characteristic impedance, there may be inductive coupling depending on the space between the conductor lines [29].

C.1 Cross-talk calculation

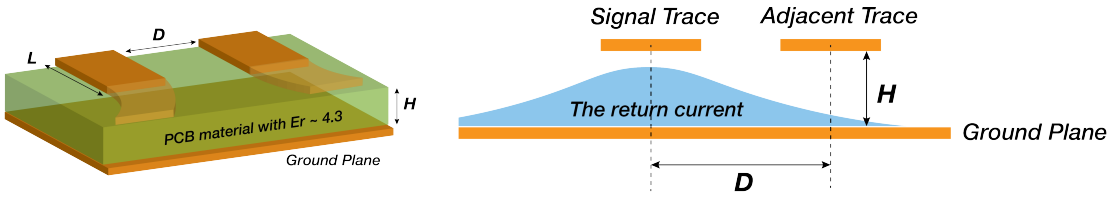


Figure C.1: The return current density on the ground plane, when a high speed signal propagates on a signal trace.

When a high speed signal propagates on a signal trace, the return current density $i(D)$ at point D (as shown in Fig. C.1) is proportional to the ratio between D and H [39].

$$i(D) = \frac{I_0}{\pi H} \frac{1}{1 + \left(\frac{D}{H}\right)^2} \propto \frac{1}{1 + \left(\frac{D}{H}\right)^2} \tag{C.1}$$

Since the return current density and the associated magnetic field drops off according to Equation C.1, the cross-talk at point D is,

$$\text{Cross-talk} = \frac{V_{cross-talk}}{V_0} \propto \frac{1}{1+\left(\frac{D}{H}\right)^2} \approx \frac{K}{1+\left(\frac{D}{H}\right)^2} \tag{C.2}$$

The proportional constant K will depend on the rise-time[1] T_R of signals, and round trip propagation time T_{RT} (a function of parallel length L of the traces). Round trip propagation time T_{RT} [20] is given by,

$$T_{RT} = 1.017\sqrt{0.475\varepsilon_r + 0.67} \times \frac{2L}{c} \tag{C.3}$$

c is the speed of light in vacuum. The term $1.017\sqrt{0.475\varepsilon_r + 0.67}$ is the inverse of the speed of signals on a PCB trace (which is c/ε_{eff} and $\varepsilon_{eff} = 0.475\varepsilon_r + 0.67$).

Cross-talk increases with the length L of the parallel coupling, and reaches a maximum when T_R equals T_{RT} [40]. Hence we have for,

1. When $T_{RT}/T_R \leq 1$, the cross-talk is proportional to T_{RT}/T_R and,

$$\frac{V_{cross-talk}}{V_0} = \frac{1}{1+\left(\frac{D}{H}\right)^2}\frac{T_{RT}}{T_R} = \frac{1}{1+\left(\frac{D}{H}\right)^2}\frac{(1.017\sqrt{\varepsilon_r \cdot 0.475 + 0.67} \cdot 2L)}{c \cdot T_R} \tag{C.4}$$

2. When $T_{RT}/T_R > 1$, the cross-talk is independent of L and,

$$\frac{V_{cross-talk}}{V_0} = \frac{1}{1+\left(\frac{D}{H}\right)^2} \tag{C.5}$$

If there are terminations at both ends, the cross-talk will be reduced significantly. The new cross-talk will be proportional to reflection coefficient ρ.

$$\rho = \frac{(R_L - Z_0)}{R_L + Z_0} \tag{C.6}$$

Where Z_0 is the single-ended impedance of the line, and R_L is the termination. For small tolerances, Equation C.6 can be approximated as,

$$\rho = \frac{Tol(R_L) + Tol(Z_0)}{2} \tag{C.7}$$

[1]The rise-time of a digital signal is the time it takes to change from one state to another.

Where Tol stands for tolerance. And combining this with Equation C.4, the new cross-talk is,

$$\frac{V_{cross-talk}}{V_0} = \frac{1}{1+\left(\frac{D}{H}\right)^2} \frac{(1.017\sqrt{\varepsilon_r \cdot 0.475 + 0.67} \cdot 2L)}{c \cdot T_R} \frac{Tol(R_L) + Tol(Z_0)}{2} \tag{C.8}$$

Appendix D

Adapter Cards

D.1 4-DisplayPort data adapter card

The schematics of the 4-DisplayPort data adapter card are shown in Fig. D.1 below. As mentioned in the main text, this adapter card uses 4-DisplayPort connectors and 1 ZIF (zero insertion force) connector.

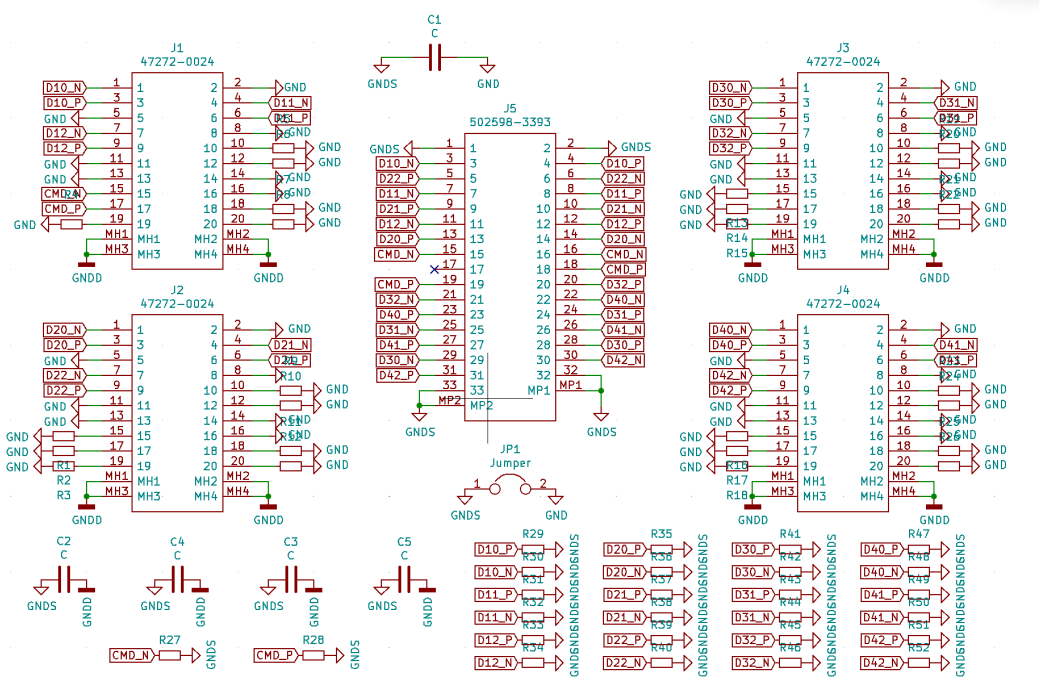


Figure D.1: The schematics of the 4-DisplayPort Data Adapter Card.

D.2 1-DisplayPort data adapter card

The schematics of the 1-DisplayPort data adapter card are shown below in Fig. D.2.

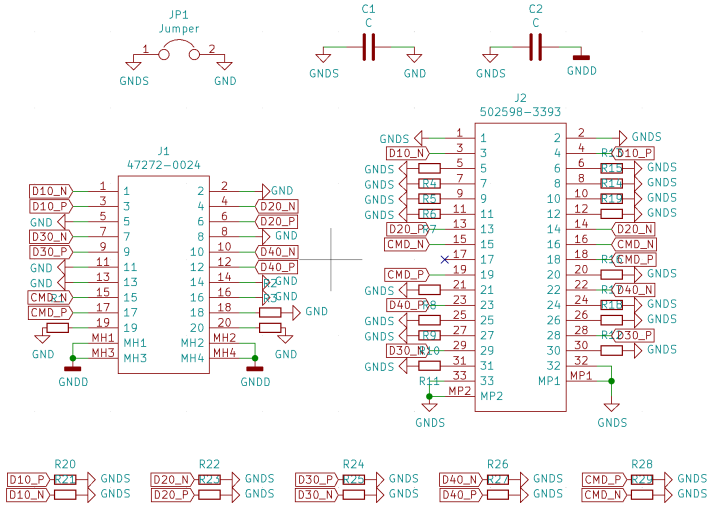


Figure D.2: The schematics of the 1-DisplayPort Data Adapter Card.

D.3 Power adapter card

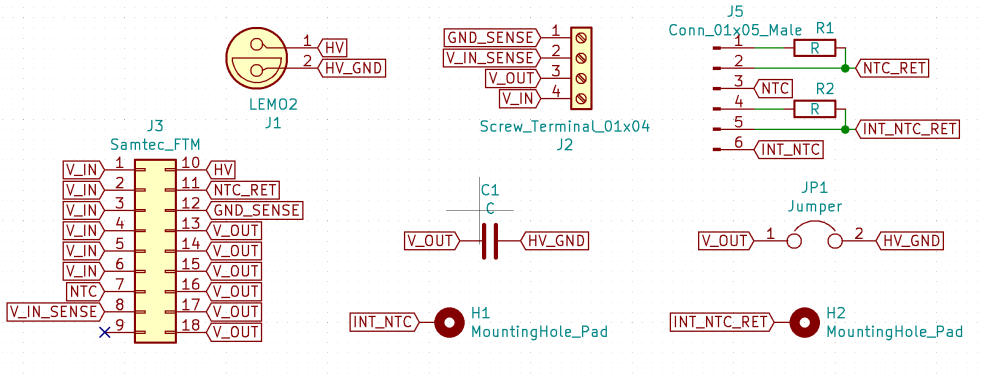


Figure D.3: The schematics of the power adapter card.

The schematics of the power adapter card, which used the components mentioned in Table 3.1, is shown in Fig. D.3.

D.4 Triplet adapter card

Although it was not discussed in this thesis, adapter cards for the triplet modules as shown in Fig. D.4 were also developed. This was developed in collaboration with LBNL (Lawrence Berkeley National Laboratories), and hence bears the LBNL logo as well. These were also produced and validated that they work without any issue.

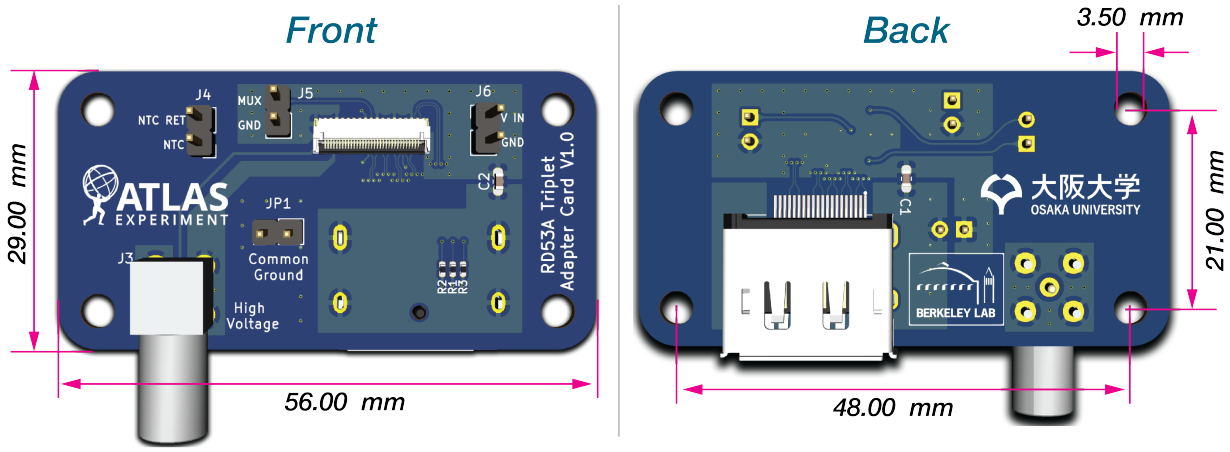


Figure D.4: The Triplet Adapter card used for testing RD53A Triplet Modules.

The Triplet Adapter card also has a LEMO connector in order to supply HV to the triplet module. However, the same power adapter card mentioned in Chapter 3, will be used for supplying low voltage to triplet modules.

D.5 Z-ray adapter card

The Z-ray adapter card, shown in Fig. D.5, bears its name from the Z-ray connector used on this adapter card. It is used for testing the ITkPixV1 Quad (the next prototype quad pixel detector) togehter with the Z-Ray Pigtail.

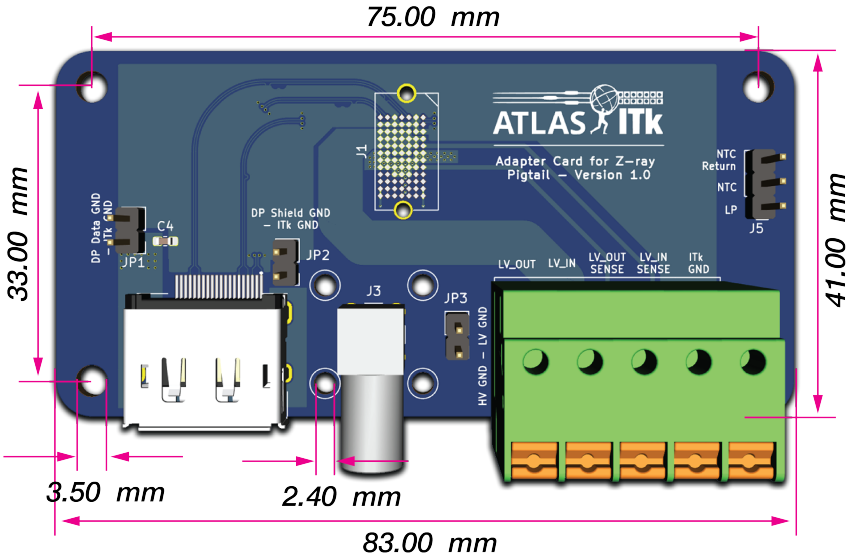


Figure D.5: The Z-ray adapter card used for testing RD53B (also known as ITkPixV1) Quad Modules together with the Z-ray pigtail.

This adapter card is still under design stage, and has not been produced yet.