大阪大学
OSAKA UNIVERSITY
HIGH ENERGY PHYSICS YAMANAKA LAB

ATLAS EXPERIMENT

YEAR END PRESENTATION 2019

Design and performance evaluation of an Adapter Board used in the mass production of new ATLAS pixel detectors for the HL-LHC

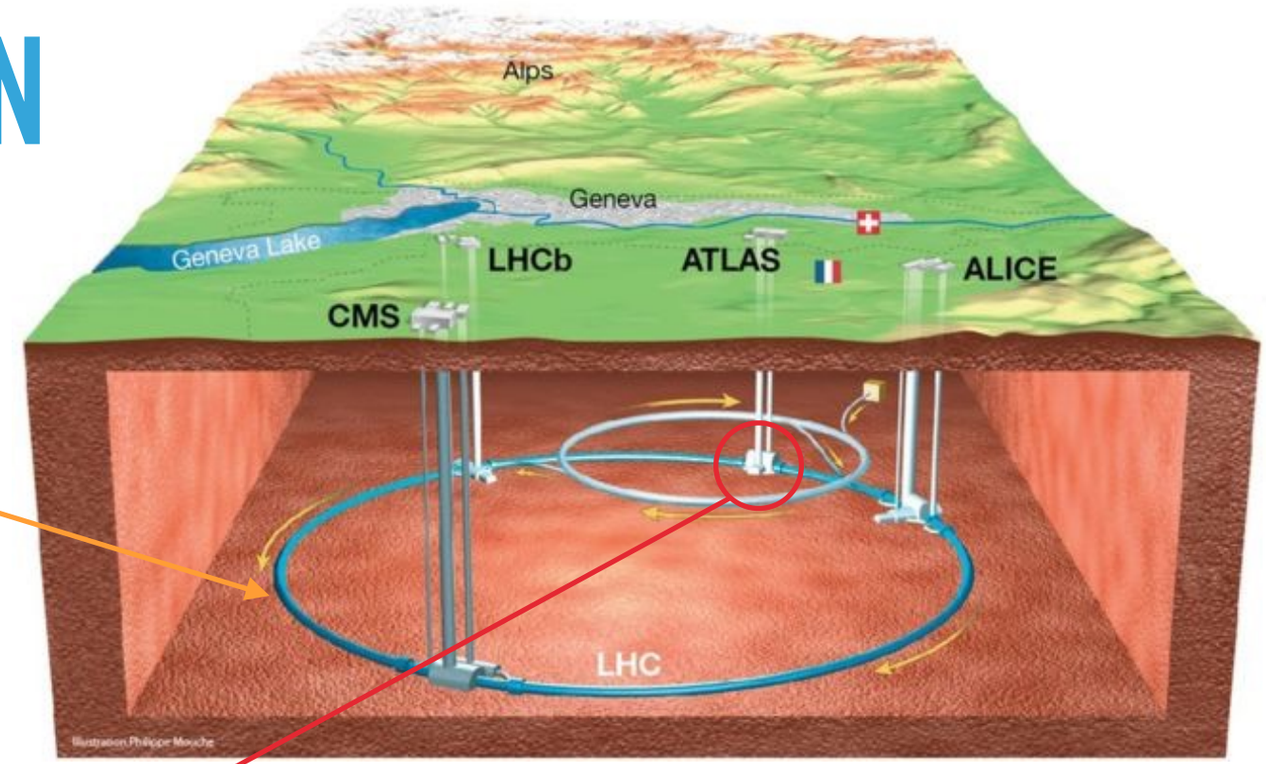
2019/12/23

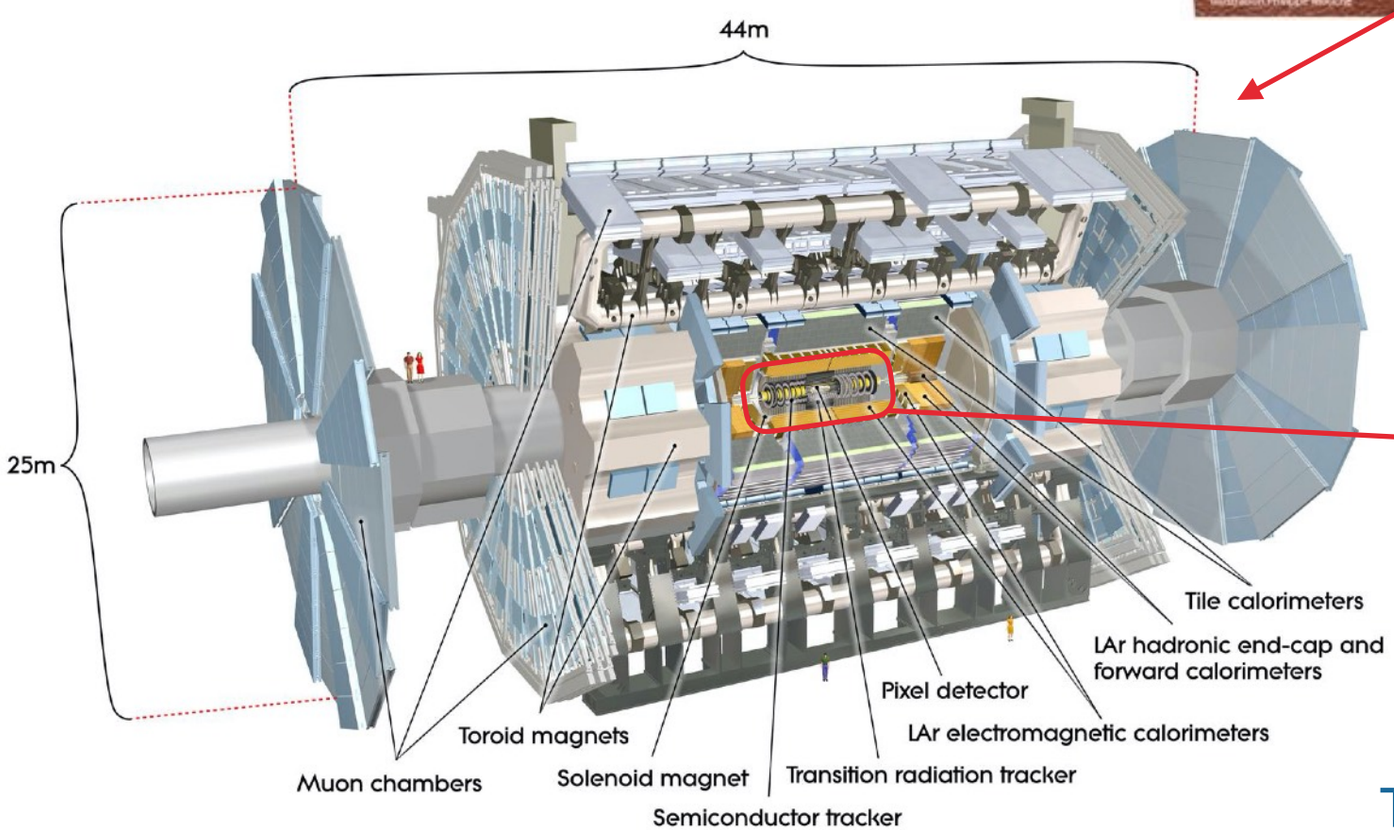
LAKMIN WICKREMASINGHE

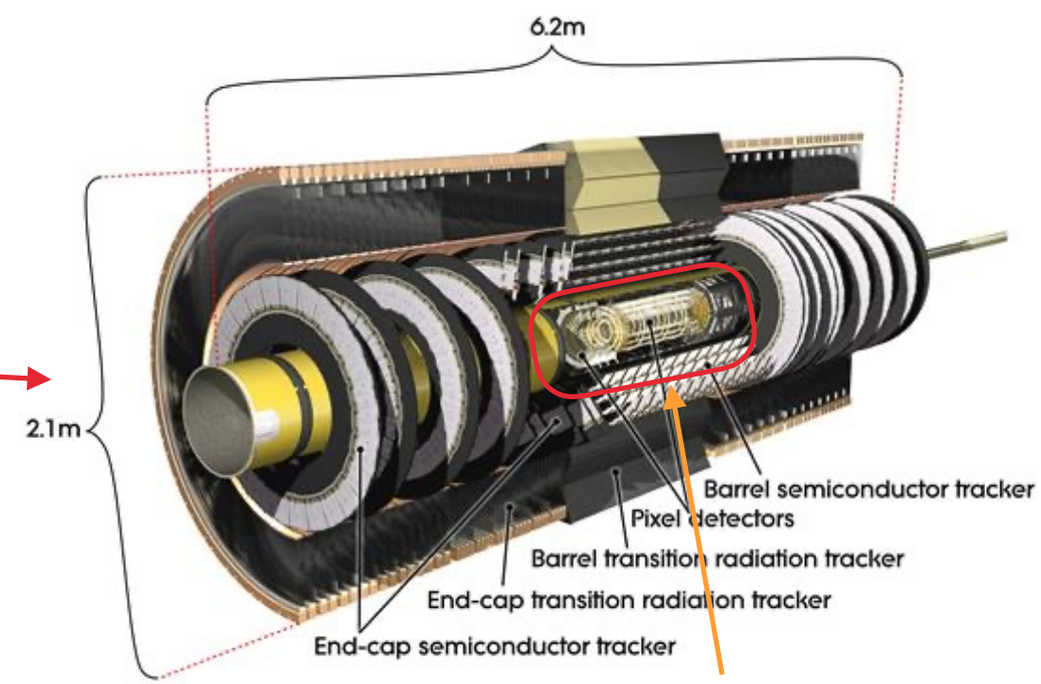
ATLAS DETECTOR – CERN

LHC ➡ High Luminosity LHC

2008 - 2024 2027 ~

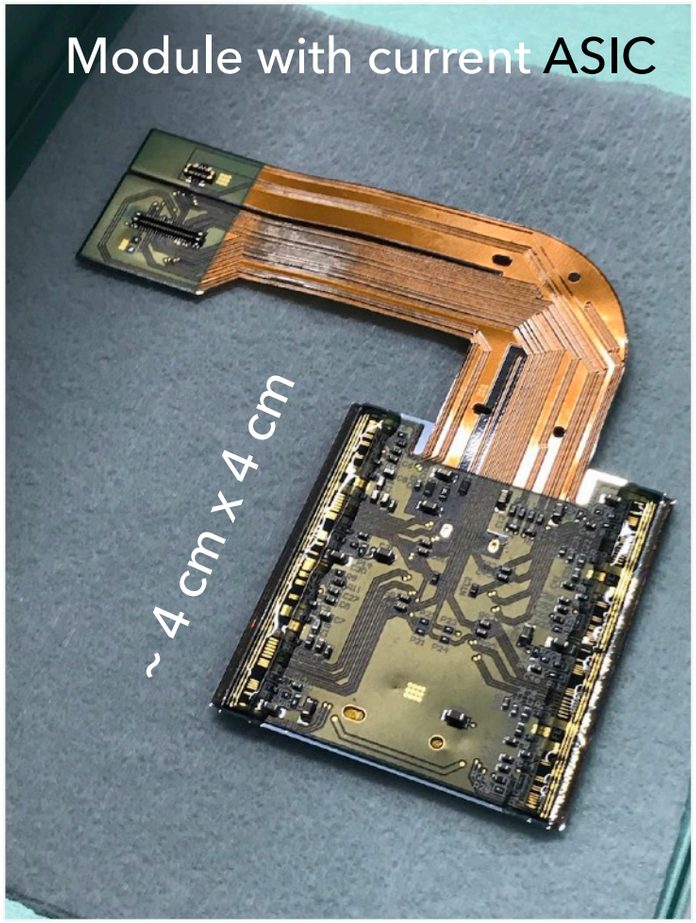


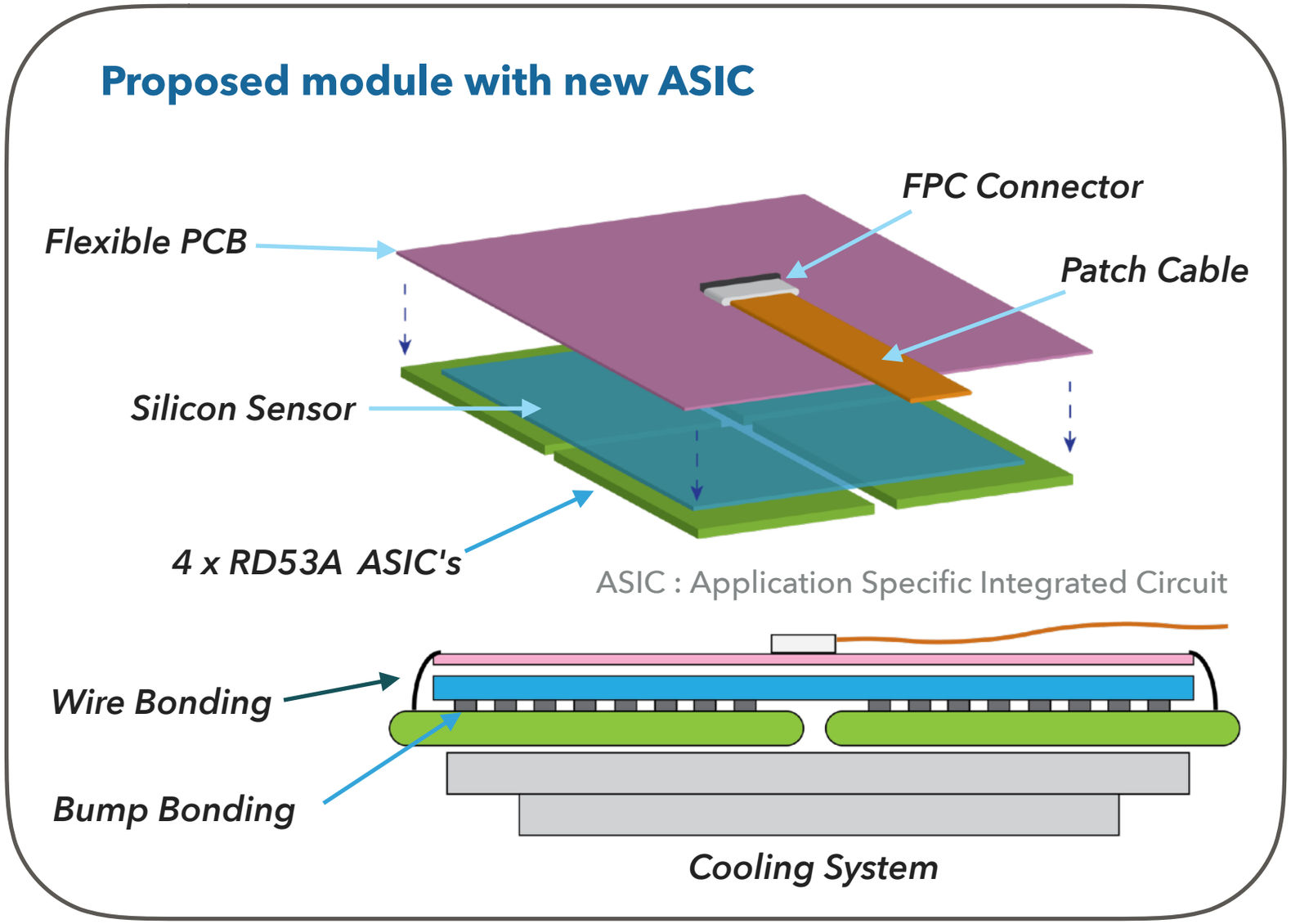




The pixels have to be replaced for HL-LHC

PIXEL MODULE





Current ASIC

Data Rate of 0.16 Gbps

Pixel Size of 50 μm X 250 μm

Trigger Rate x5

Beam Intensity x8

Compression x0.8

New ASIC

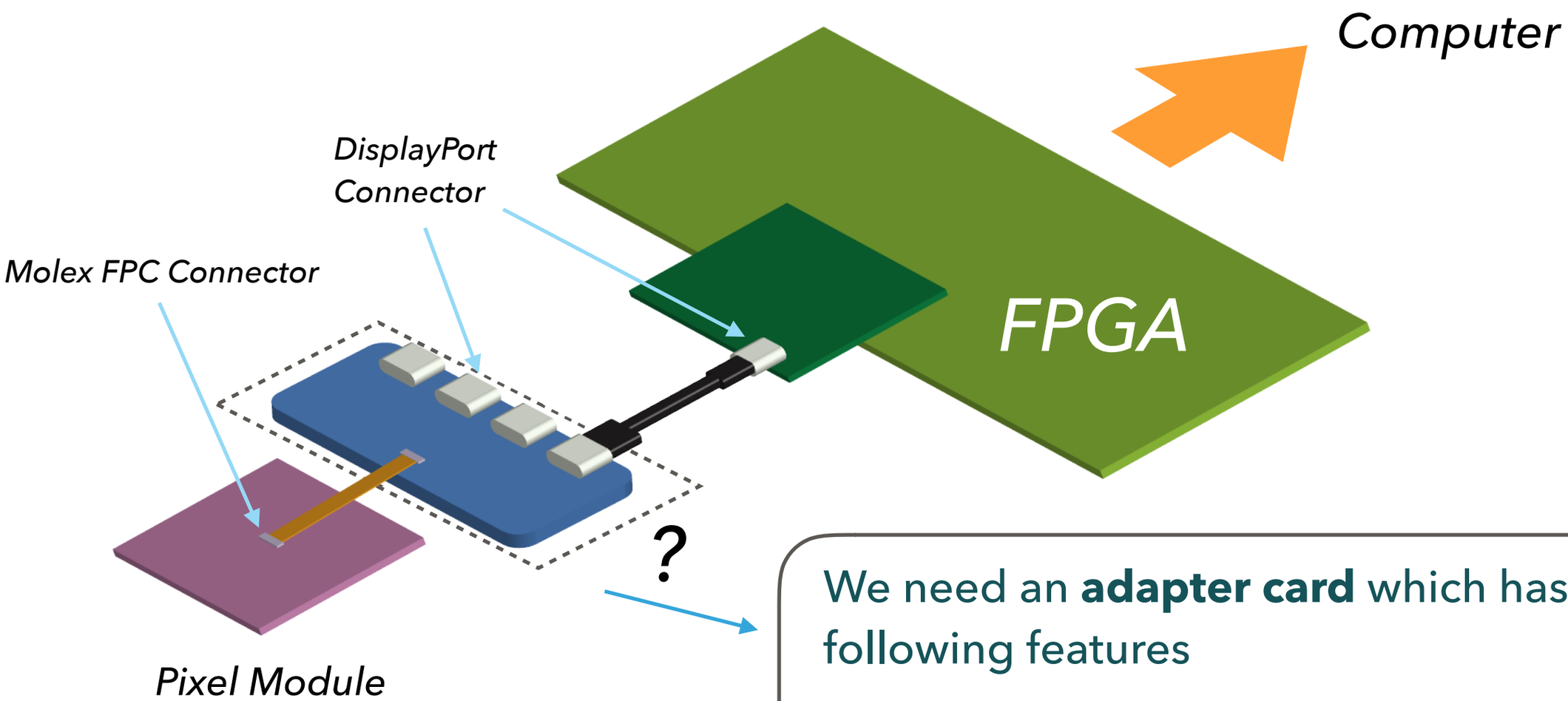
Data Rate of 5.12 Gbps

Pixel Size of 50 μm X 50 μm

QA/QC OF THE NEW MODULES

QA - Quality Assurance
QC - Quality Control

ATLAS Japan will produce ~2000 modules



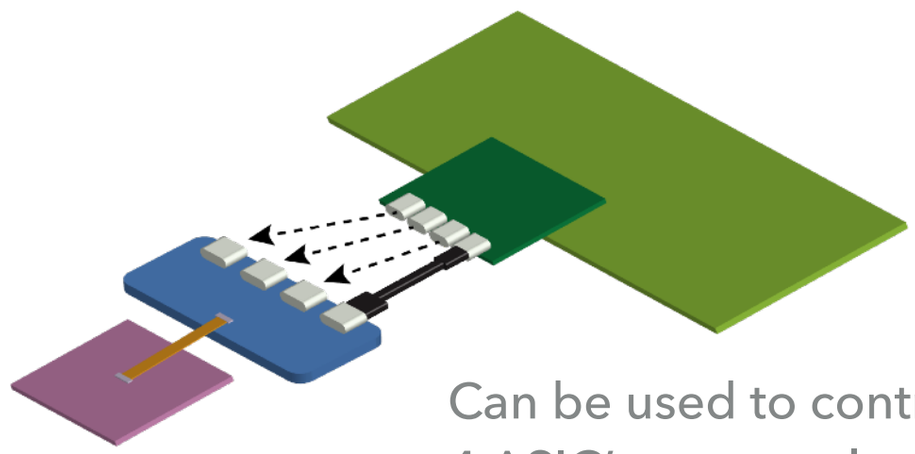
We need an **adapter card** which has the following features

- FPC Connector ➡ DisplayPort conversion
- Can transmit 1.28 Gbps
- Impedance controlled

ADAPTER CARDS

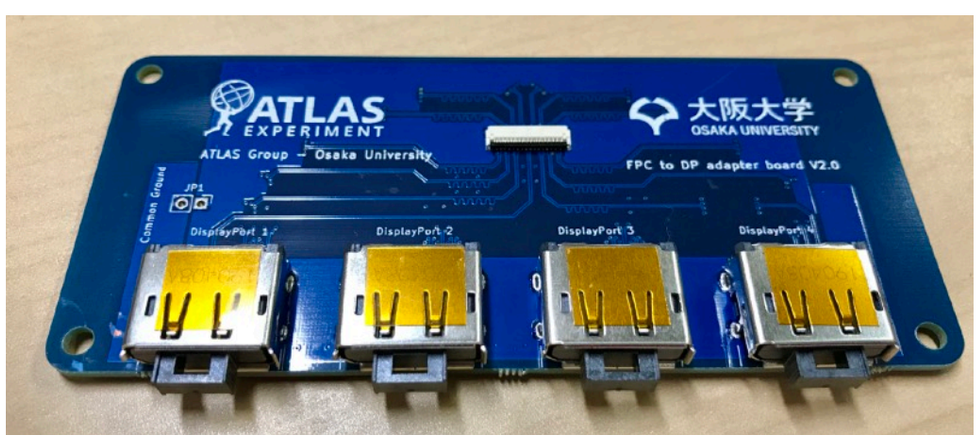
I designed 2 types of adapter cards

4 DISPLAYPORT VERSION

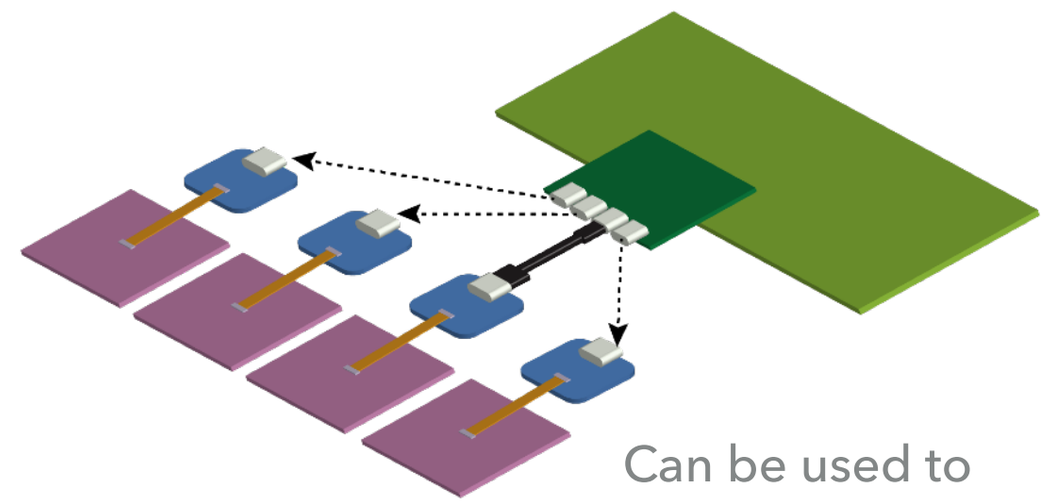


Can be used to control 4 ASIC's separately

Versions : 1.0, 2.0, 2.1

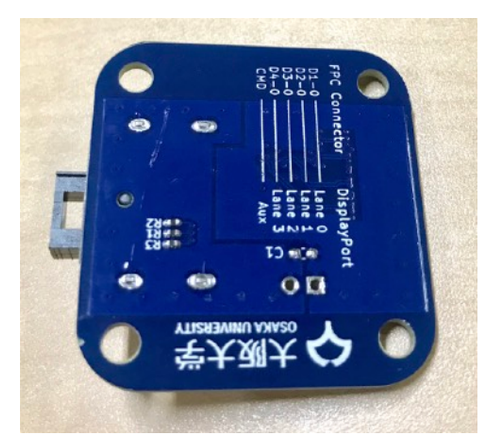


1 DISPLAYPORT VERSION



Can be used to control 4 modules

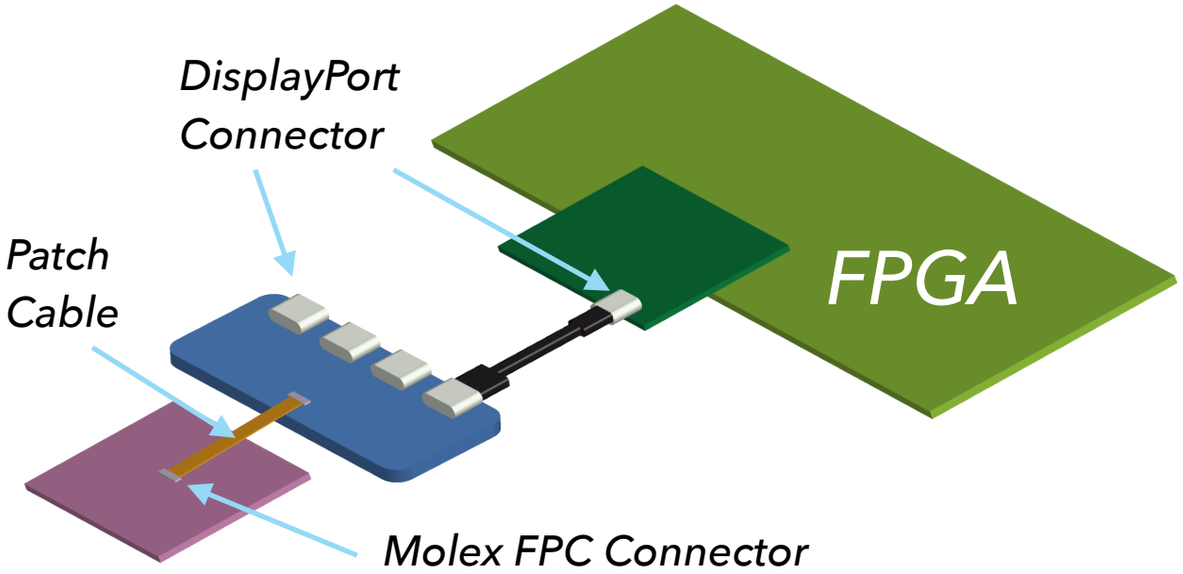
Versions : 1.0



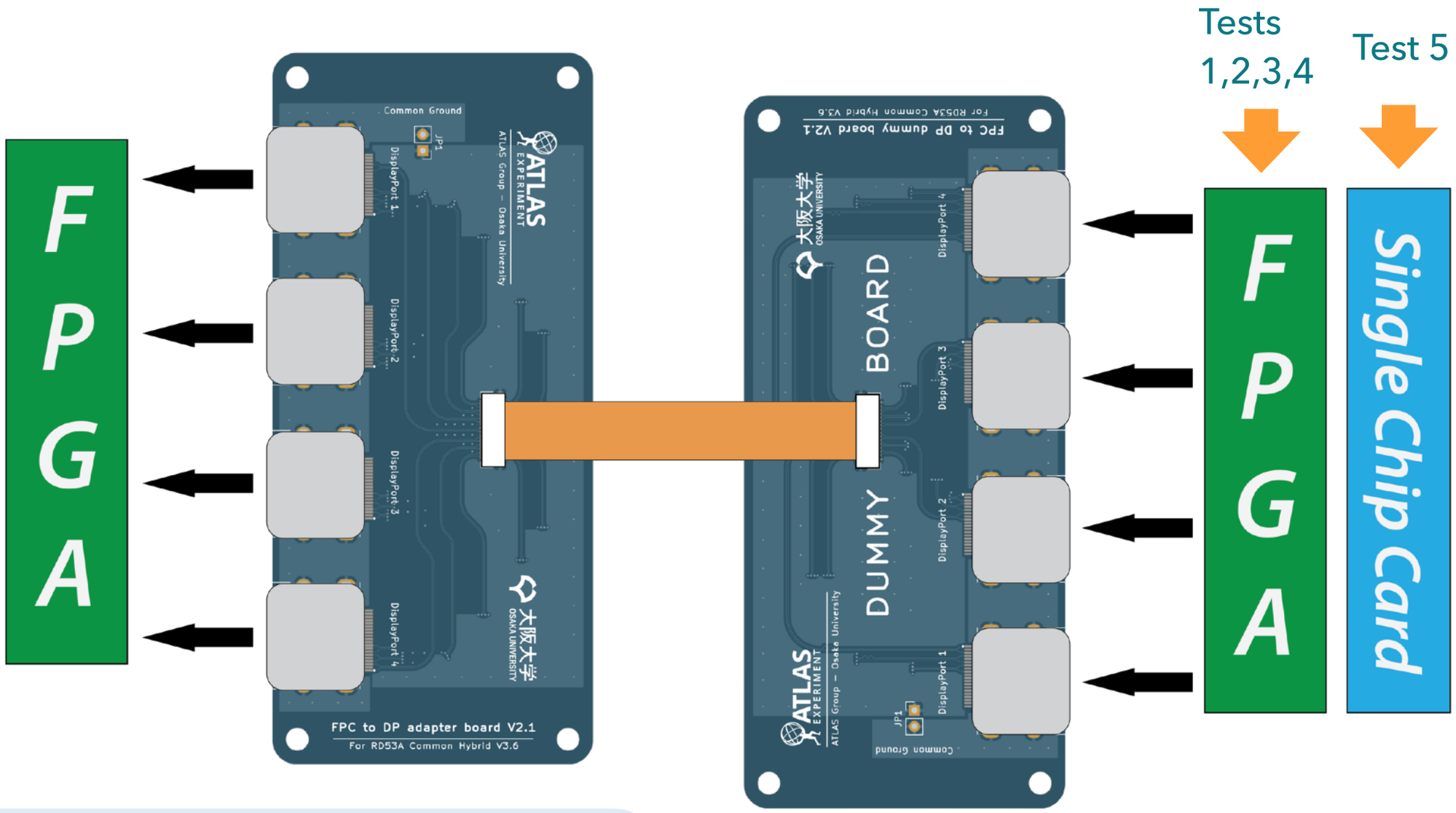
HIGH SPEED READOUT TESTS – USING 4 DP VERSION 1.0

- ✓ Test 1 - High speed readout at different data rates
- ✓ Test 2 - Mating Cycles of the patch cable & connector
- ✓ Test 3 - Patch Cable-Cable Dependance
- ✓ Test 4 - Cross-talk test (Between Data Lanes)
- ✓ Test 5 - Readout test with the Single Chip Card (SCC)

I will only talk about Test 1, Test 2, Test 5 today. Please check the backup slides for details on Test 3 and Test 4.



HIGH SPEED READOUT TESTS – SETUP



Made a Dummy Board

This will mirror the connections, so it will act as the module for the tests

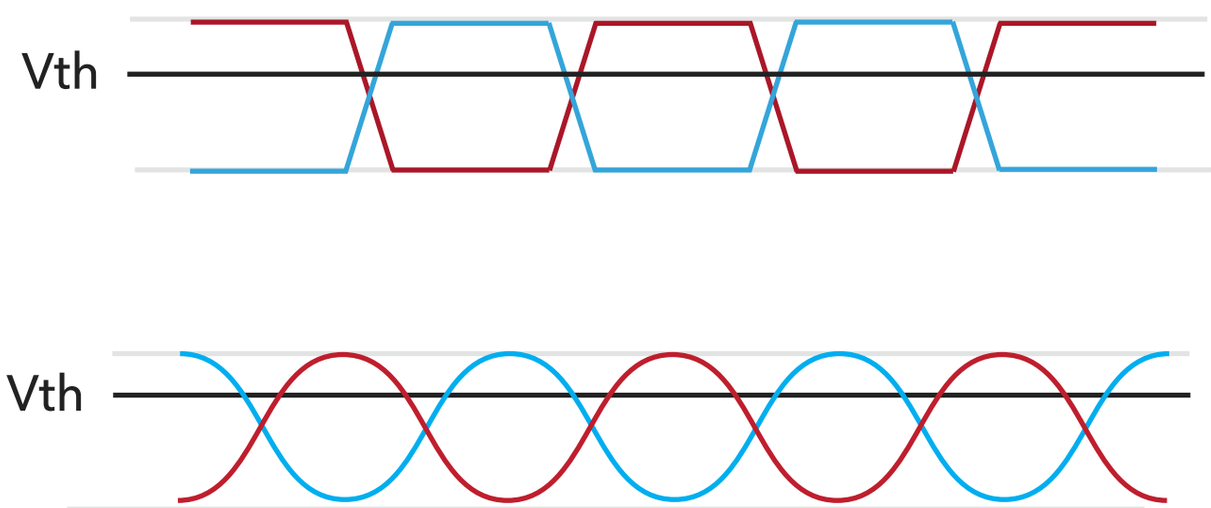
TESTING FOR HIGH SPEED READOUT – IBERT

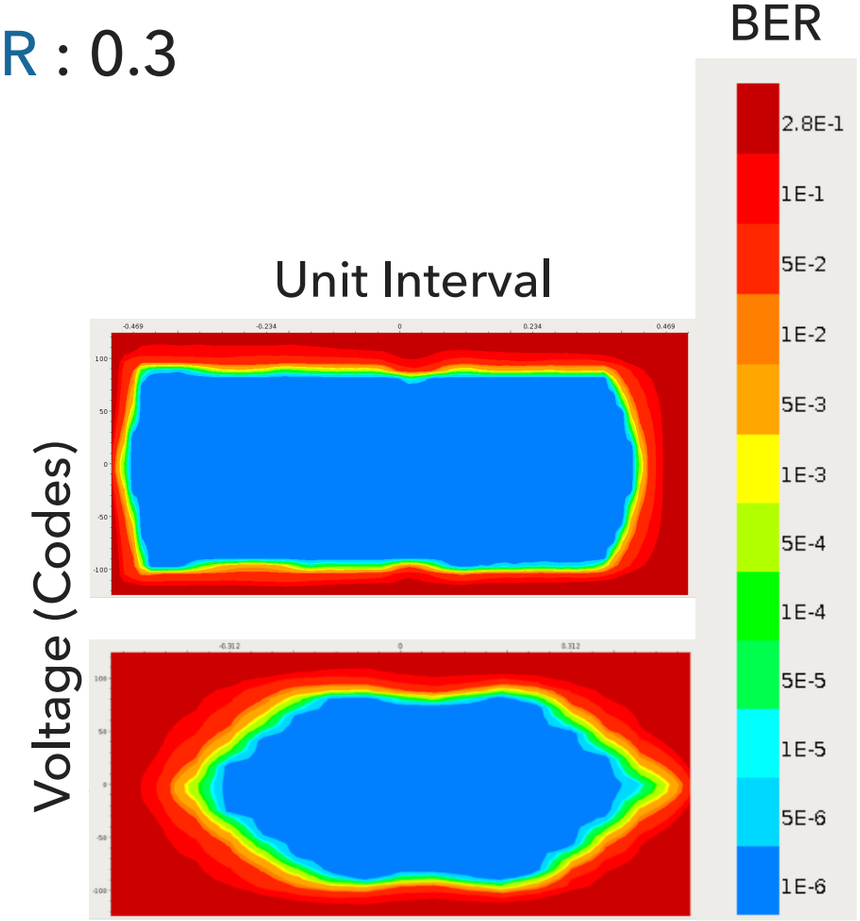
IBERT : Integrated Bit Error Ratio Test

Errors : 3 per 10 bits sent

BER : 0.3

2D-eye scan





TEST 1 – DATA SPEEDS

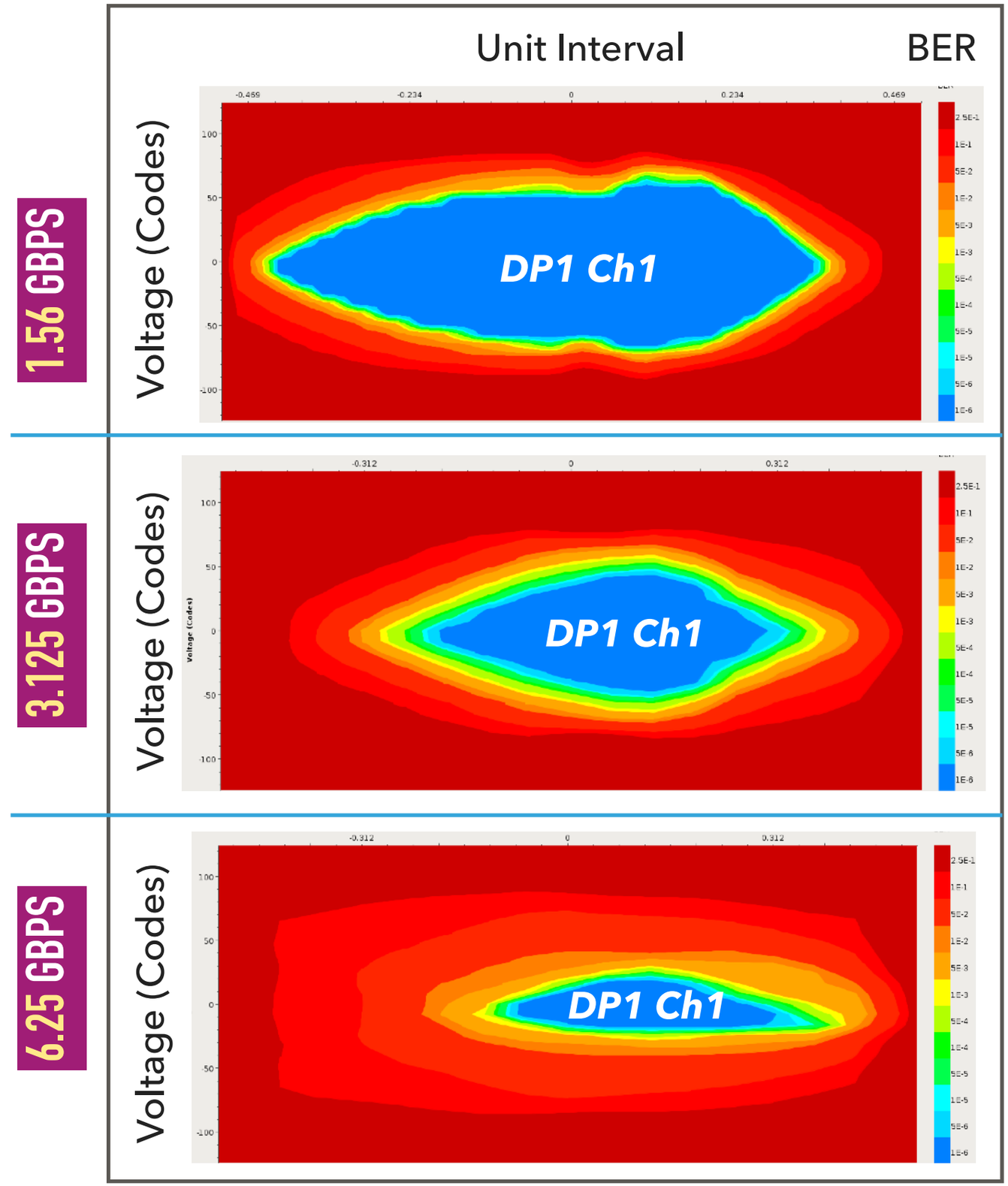
TX (P,N) to SMA to DP to FPC to RX (P,N)

- Tested at 1.56 Gbps
  - ✓ No errors
  - ✓ All channels passed

IT'S POSSIBLE TO SEND A 1.28 Gbps SIGNAL

- To check the upper limit, tested at 6.25 Gbps
  - 2 channels didn't pass

Please check backup slides for more details



TEST 2 – MATING CYCLES

Quality Assurance and Control for ~2000 modules

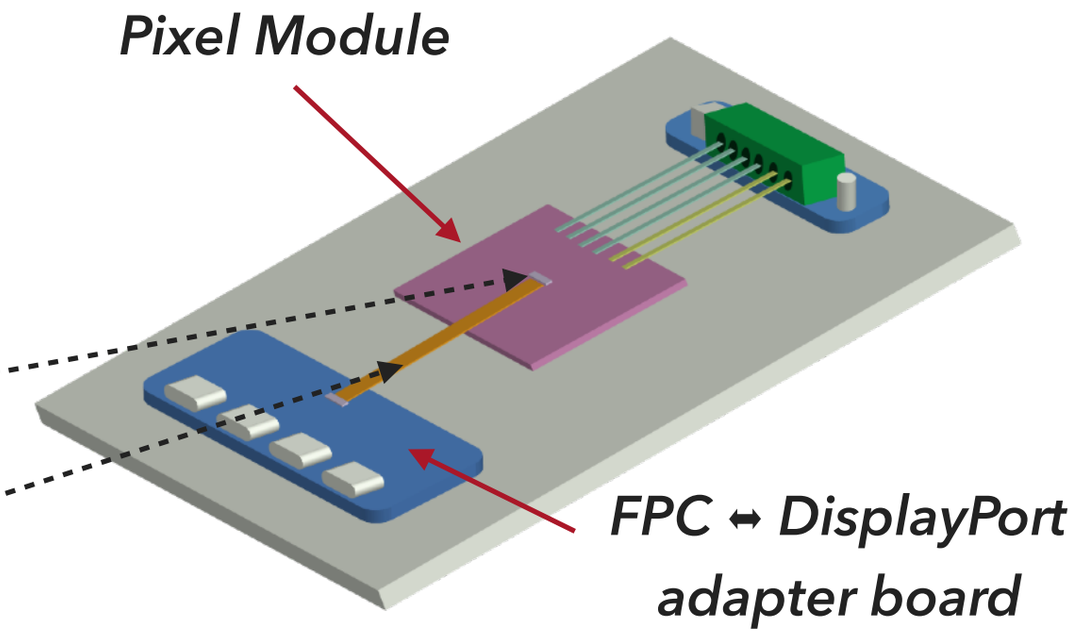
To keep the contact resistance below 60 Ω

FPC Connector

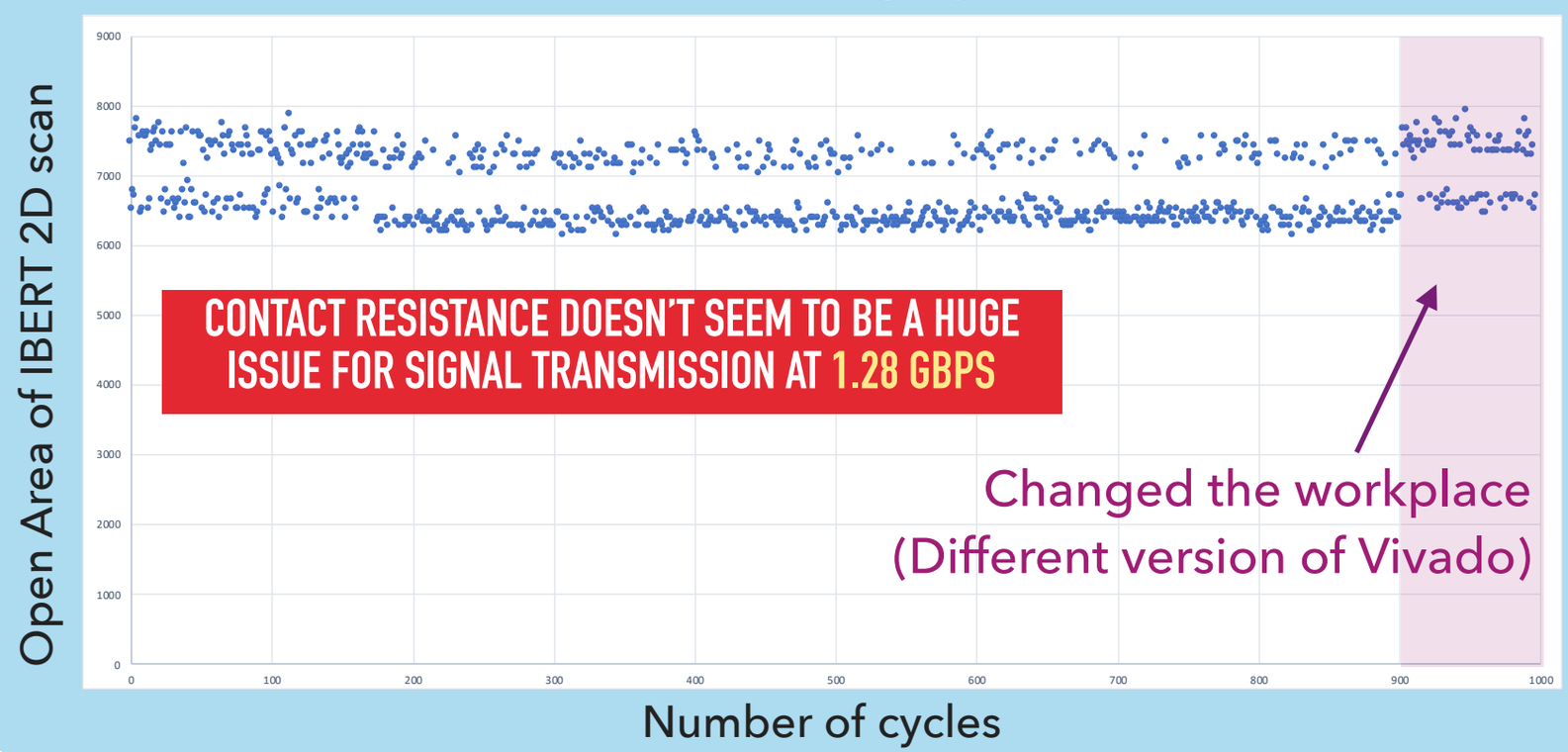
- *Molex ⟶ ~10 times*
- *JAE ⟶ ~20 times*

Patch Cable

- *Abrasion ⟶ ~1000 times*
- *Bending ⟶ ~20 times*

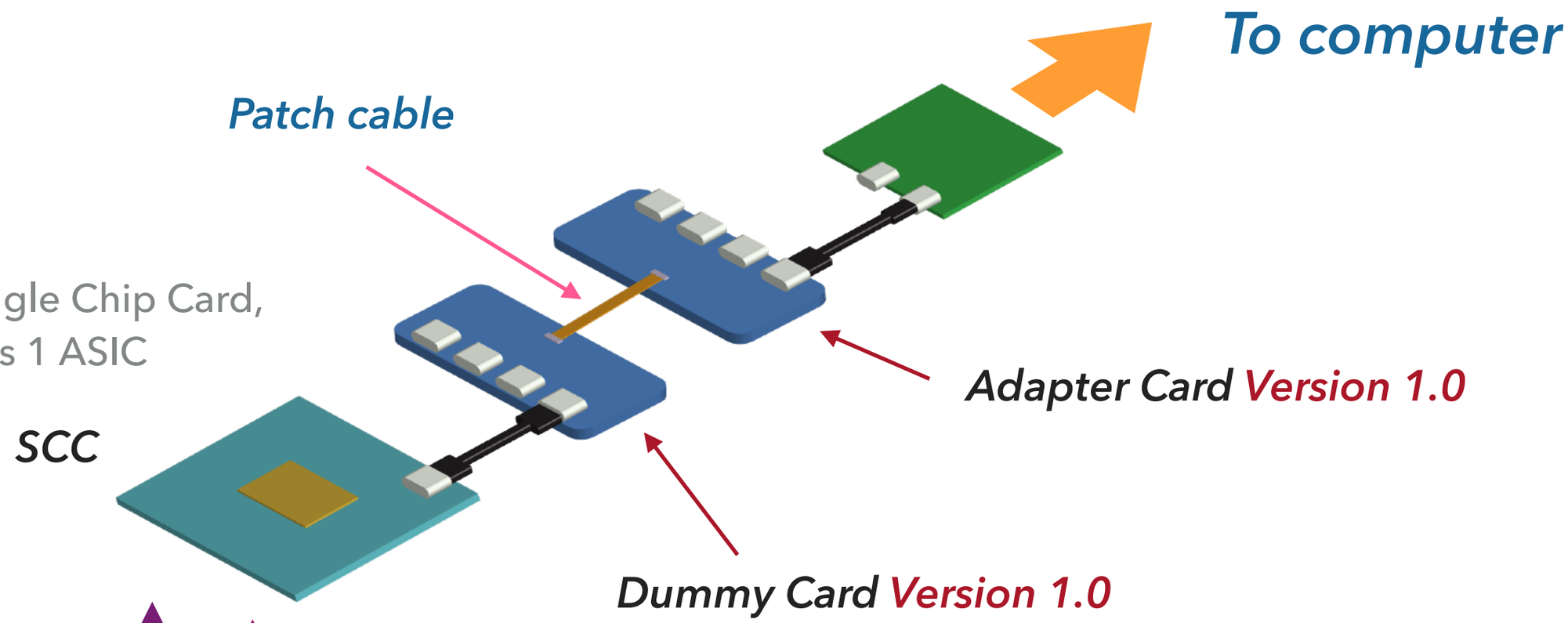


1000 times mating cycle Result



The open area hasn't changed much! The connector + cable is still good.

TEST 5 – READOUT TEST WITH SCC



SCC : Single Chip Card, which has 1 ASIC

Regulator Powered ?

Directly Powered ✓

Check backup slides for details

SUMMARY & FUTURE PLAN

Summary

- Designed an adapter card which can transmit data at 1.28 Gbps, and conducted several data transmission test with it
- Performed several tests to make sure the connectors and cables are durable for multiple tests
- Performed scans to identify optimum voltage regions where the RD53A ASIC can be operated properly

Future Plan

- Distribute ~40 boards (1 DP and 4 DP) to tests sites across the world
- Develop FPGA firmware which is needed to operate different boards in the future

BACK UP

TEST 3 – CABLE-CABLE DEPENDANCE

SHORT PATCH CABLE

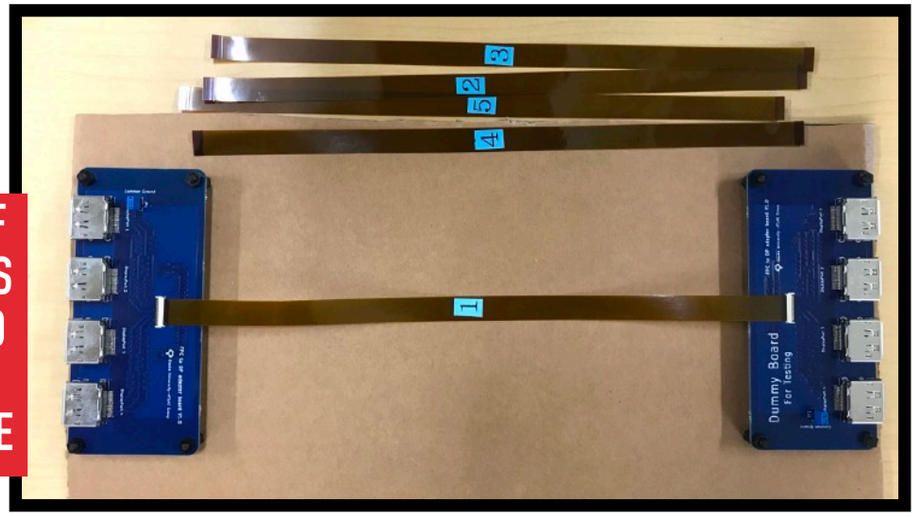
Cable	Average	Std.Dev
1	7677	221
2	6841	214
3	6835	239
4	6893	191
5	6950	343

Model Number : 150150433 Length : 10.16 cm

LONG PATCH CABLE

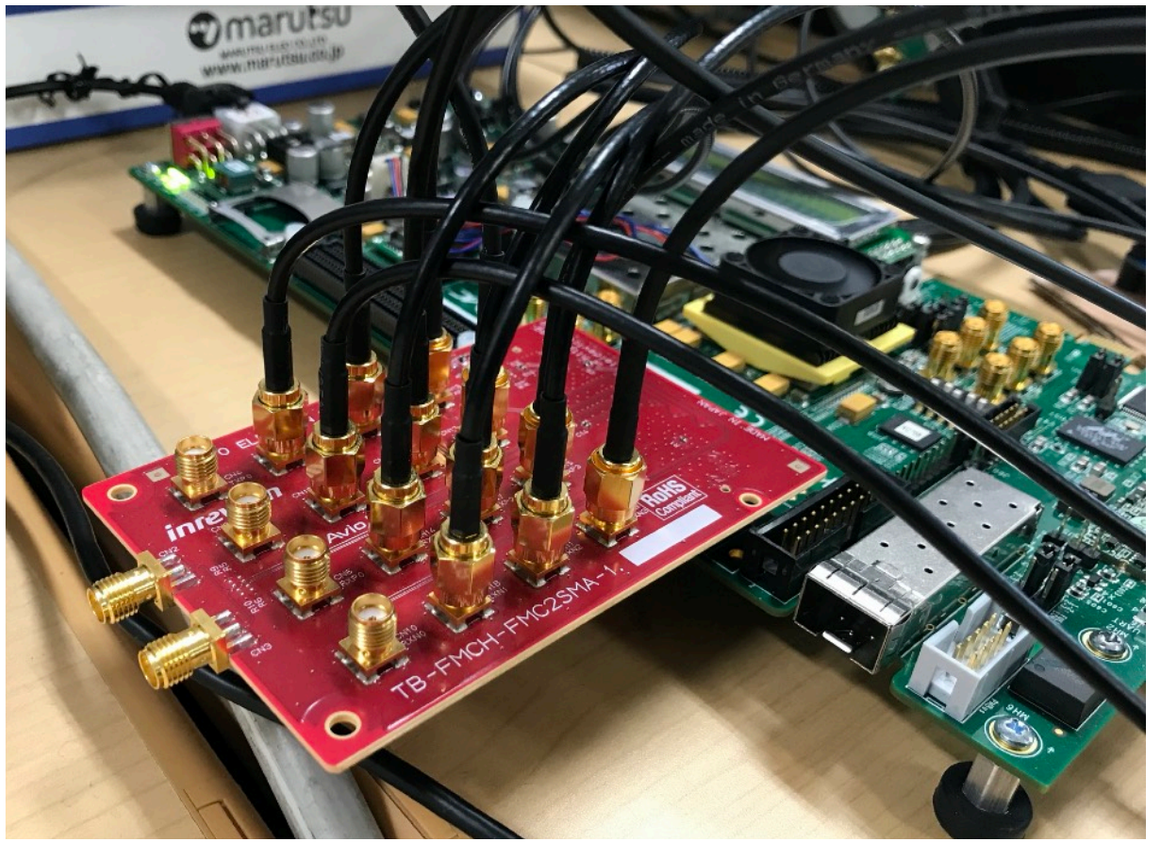
Cable	Average	Std.Dev
1	6042	285
2	6285	307
3	5619	243
4	5734	396
5	5734	272

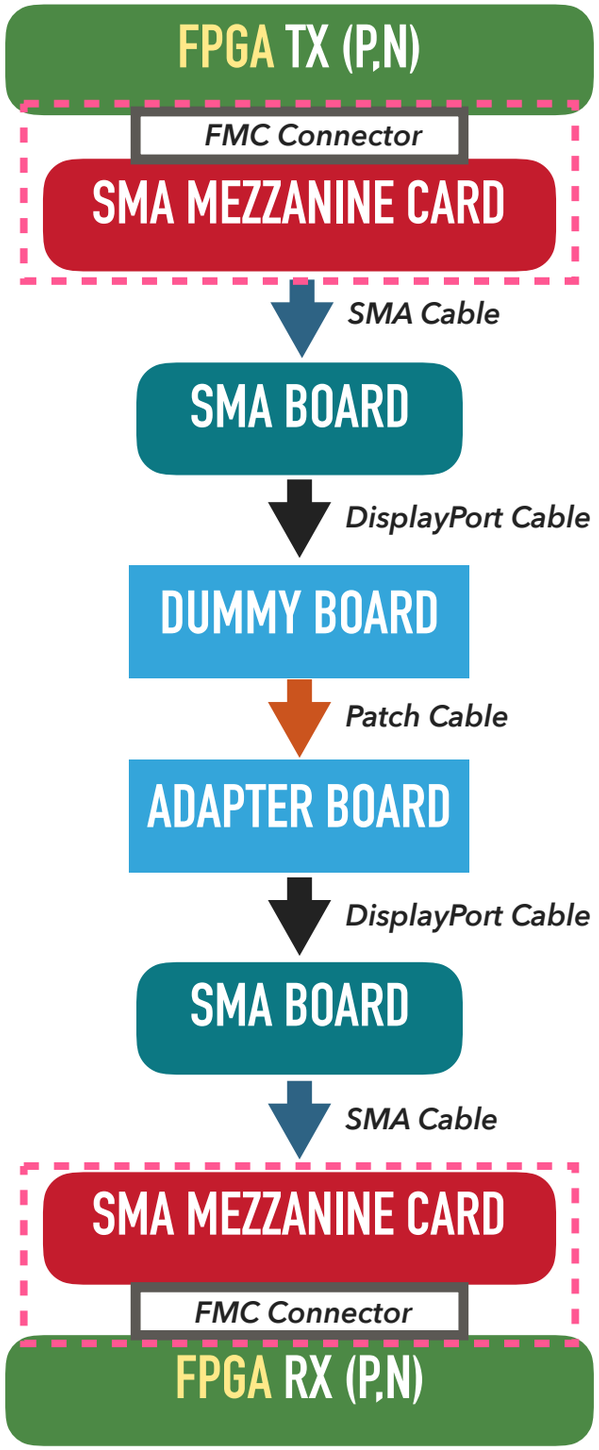
THE SIZE OF THE EYE HAS DECREASED FOR THE LONG CABLE



Model Number : 150151033 Length : 25.4 cm

CROSS-TALK TEST





- Measured BER at 1.953 Gbps

TEST 4 – CROSSTALK

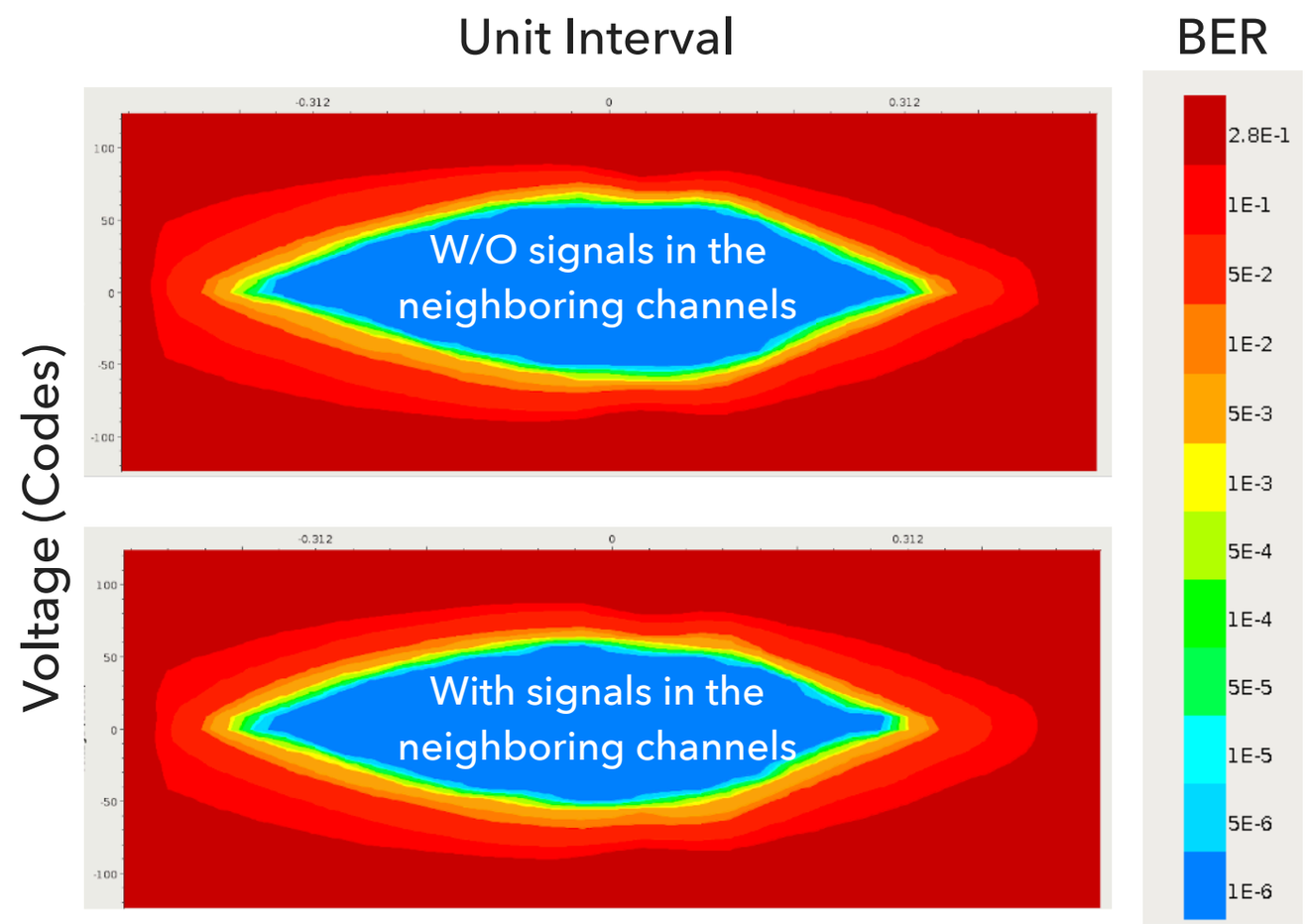
- Measured BER at 1.953 Gbps for 10 times
- Measured BER for DP1 Channel 2

Cross-talk	Average	Std.Dev
With	11002	119
Without	12320	110

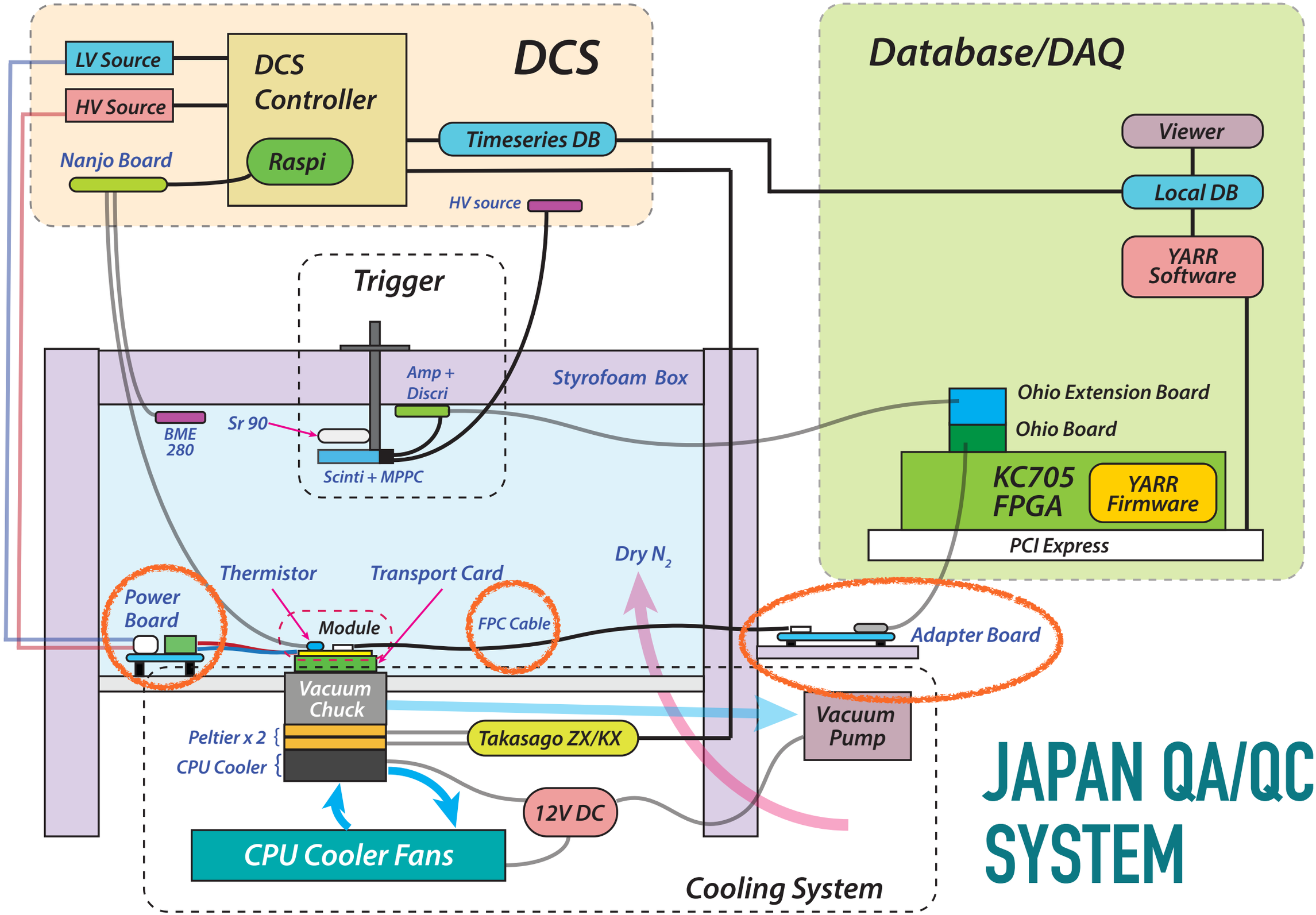
Channel 1 **Channel 2** **Channel 3**

10 % reduction in the open area

Channel 1 **Channel 2** **Channel 3**



NO SIGNIFICANT ISSUE FROM CROSS TALK FOR SIGNAL TRANSMISSION AT 1.28 GBPS



JAPAN QA/QC SYSTEM

DIRECTLY POWERED OHIO ➡ DUMMY ➡ DUMMY ➡ SCC VOLTAGE SCAN 2D GRAPH

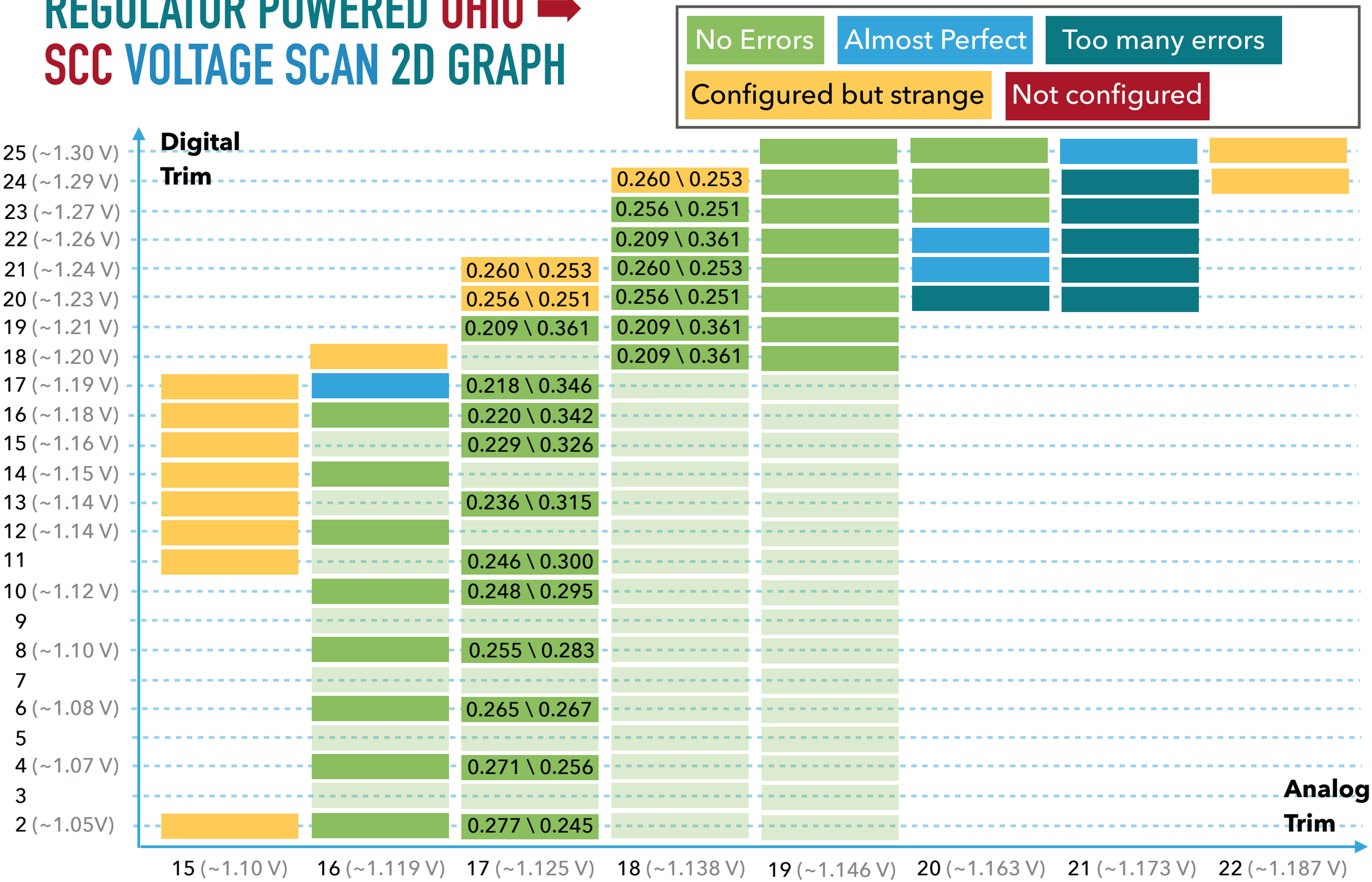
No Errors | Almost Perfect | Too many errors | Configured but YARR doesn't work | Not configured

VDDA \ VDDD	1.23 V	1.24 V	1.25 V	1.26 V	1.27 V	1.28 V	1.29 V	1.30 V
1.25 V							A : 0.244 A D : 0.331 A	A : 0.240 A D : 0.338 A
1.24 V						A : 0.243 A D : 0.329 A	A : 0.238 A D : 0.335 A	A : 0.234 A D : 0.342 A
1.23 V					A : 0.241 A D : 0.326 A	A : 0.237 A D : 0.332 A	A : 0.233 A D : 0.339 A	A : 0.229 A D : 0.346 A
1.22 V				A : 0.239 A D : 0.323 A	A : 0.235 A D : 0.330 A	A : 0.231 A D : 0.337 A	A : 0.227 A D : 0.343 A	A : 0.223 A D : 0.350 A
1.21 V			A : 0.237 A D : 0.320 A	A : 0.233 A D : 0.327 A	A : 0.229 A D : 0.333 A	A : 0.225 A D : 0.340 A	A : 0.222 A D : 0.347 A	
1.20 V		A : 0.235 A D : 0.317 A	A : 0.232 A D : 0.324 A	A : 0.228 A D : 0.330 A	A : 0.224 A D : 0.337 A	A : 0.220 A D : 0.344 A		
1.19 V	A : 0.227 A D : 0.294 A	A : 0.230 A D : 0.321 A	A : 0.226 A D : 0.327 A	A : 0.216 A D : 0.313 A				

A : VDDA Current

D : VDDD Current

REGULATOR POWERED OHIO ➡ SCC VOLTAGE SCAN 2D GRAPH



DEFINITION OF REGIONS – VOLTAGE SCAN

Too many errors

```
18936 [5] Received data not valid: [14637,18936] = 0xdd7cf1ff
18936 [5] Received data not valid: [14639,18936] = 0x4dfcf9ef
 ---> Mask Stage 15
21196 [5] Received data not valid: [1259,21196] = 0x1913f01
21104 [5] Received data not valid: [11365,21104] = 0xd93ff9ff
21104 [5] Received data not valid: [11370,21104] = 0x85cfff8f
21104 [5] Received data not valid: [14441,21104] = 0xd83ff9ff
 ---> Mask Stage 16
21760 [5] Received data not valid: [12613,21760] = 0x1b1c483
21764 [5] Received data not valid: [6244,21764] = 0x35b19fff
 ---> Mask Stage 17
21754 [5] Received data not valid: [3463,21754] = 0x1911869
21732 [5] Received data not valid: [1,2] = 0xe5e00000
 ---> Mask Stage 18
21764 [5] Received data not valid: [9029,21764] = 0xd155f79f
 ---> Mask Stage 19
21562 [5] Received data not valid: [15188,21562] = 0xe4c7e9ff
19038 [5] Received data not valid: [17312,19038] = 0x9da7ffc1
 ---> Mask Stage 20
21108 [5] Received data not valid: [19181,21108] = 0x41e9fff9
 ---> Mask Stage 21
19372 [5] Received data not valid: [13029,19372] = 0xd16bfff9
21158 [5] Received data not valid: [7122,21158] = 0xe06bfff9
 ---> Mask Stage 22
20424 [5] Received data not valid: [11835,20424] = 0xd0edf7f9
19502 [5] Received data not valid: [7565,19502] = 0xec55a762
 ---> Mask Stage 23
21200 [5] Received data not valid: [14142,21200] = 0xcd7e9fff
17554 [5] Received data not valid: [13892,17554] = 0x81dfff9f
 ---> Mask Stage 24
21046 [5] Received data not valid: [2149,21046] = 0x1a1ecaa
21046 [5] Received data not valid: [2841,21046] = 0xe020ff9f
 ---> Mask Stage 25
21558 [5] Received data not valid: [4351,21558] = 0xa1839fff
21558 [5] Received data not valid: [4357,21558] = 0xdc32fff9
21768 [5] Received data not valid: [17447,21768] = 0xd432f7f9
19022 [5] Received data not valid: [8126,19022] = 0x89e3ff9f
 ---> Mask Stage 26
19000 [5] Received data not valid: [11726,19000] = 0x3185ff83
19000 [5] Received data not valid: [18584,19000] = 0x5994f9cf
 ---> Mask Stage 27
21718 [5] Received data not valid: [18992,21718] = 0x81e7ff9f
```

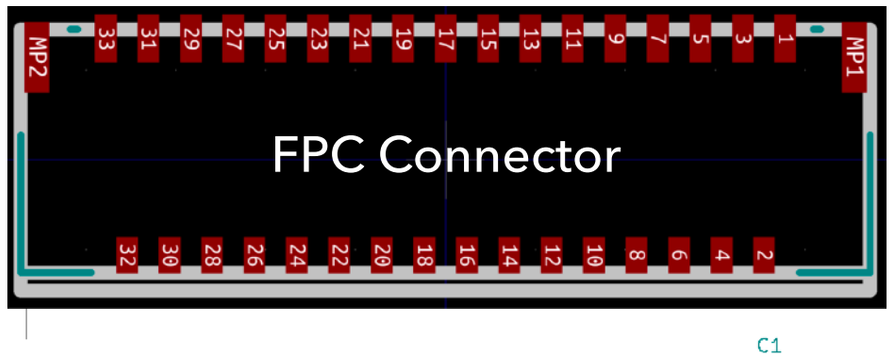
Almost Perfect

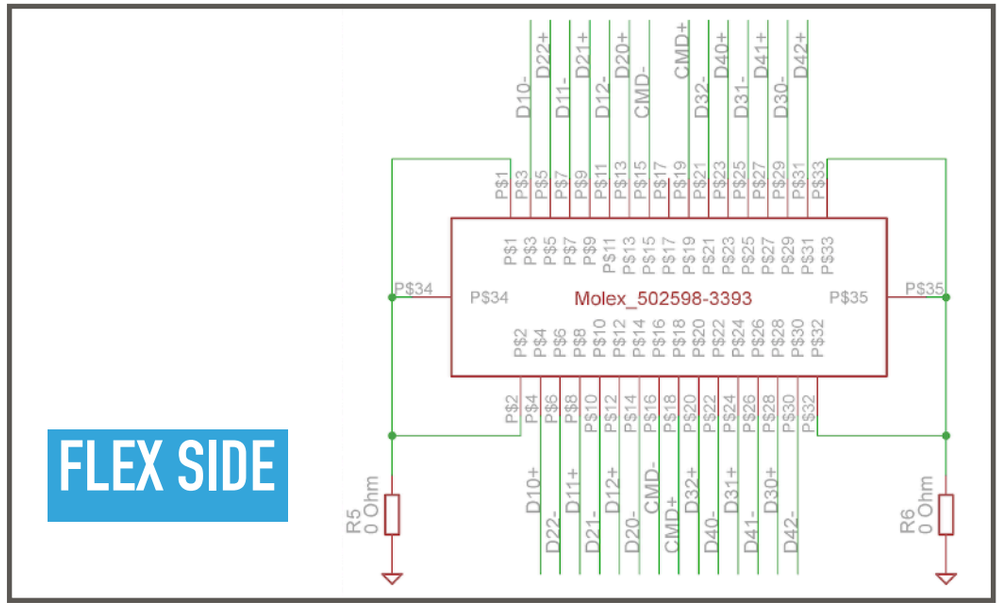
```
 ---> Mask Stage 31
 ---> Mask Stage 32
 ---> Mask Stage 33
 ---> Mask Stage 34
 ---> Mask Stage 35
 ---> Mask Stage 36
 ---> Mask Stage 37
 ---> Mask Stage 38
 ---> Mask Stage 39
 ---> Mask Stage 40
 ---> Mask Stage 41
 ---> Mask Stage 42
 ---> Mask Stage 43
 ---> Mask Stage 44
 ---> Mask Stage 45
21200 [5] Received data not valid: [20008,21200] = 0x85baf9df
 ---> Mask Stage 46
 ---> Mask Stage 47
 ---> Mask Stage 48
 ---> Mask Stage 49
 ---> Mask Stage 50
 ---> Mask Stage 51
 ---> Mask Stage 52
 ---> Mask Stage 53
 ---> Mask Stage 54
 ---> Mask Stage 55
 ---> Mask Stage 56
 ---> Mask Stage 57
 ---> Mask Stage 58
 ---> Mask Stage 59
 ---> Mask Stage 60
 ---> Mask Stage 61
 ---> Mask Stage 62
 ---> Mask Stage 63
-> Scan done!
-> Waiting for processors to finish ...
-> Processor done, waiting for histogrammer ...
virtual void Fei4Histogrammer::process(): processorDone!
-> Processor done, waiting for analysis ...
virtual void Fei4Analysis::process(): histogrammerDone!
void Fei4Analysis::end()
-> All done!
```

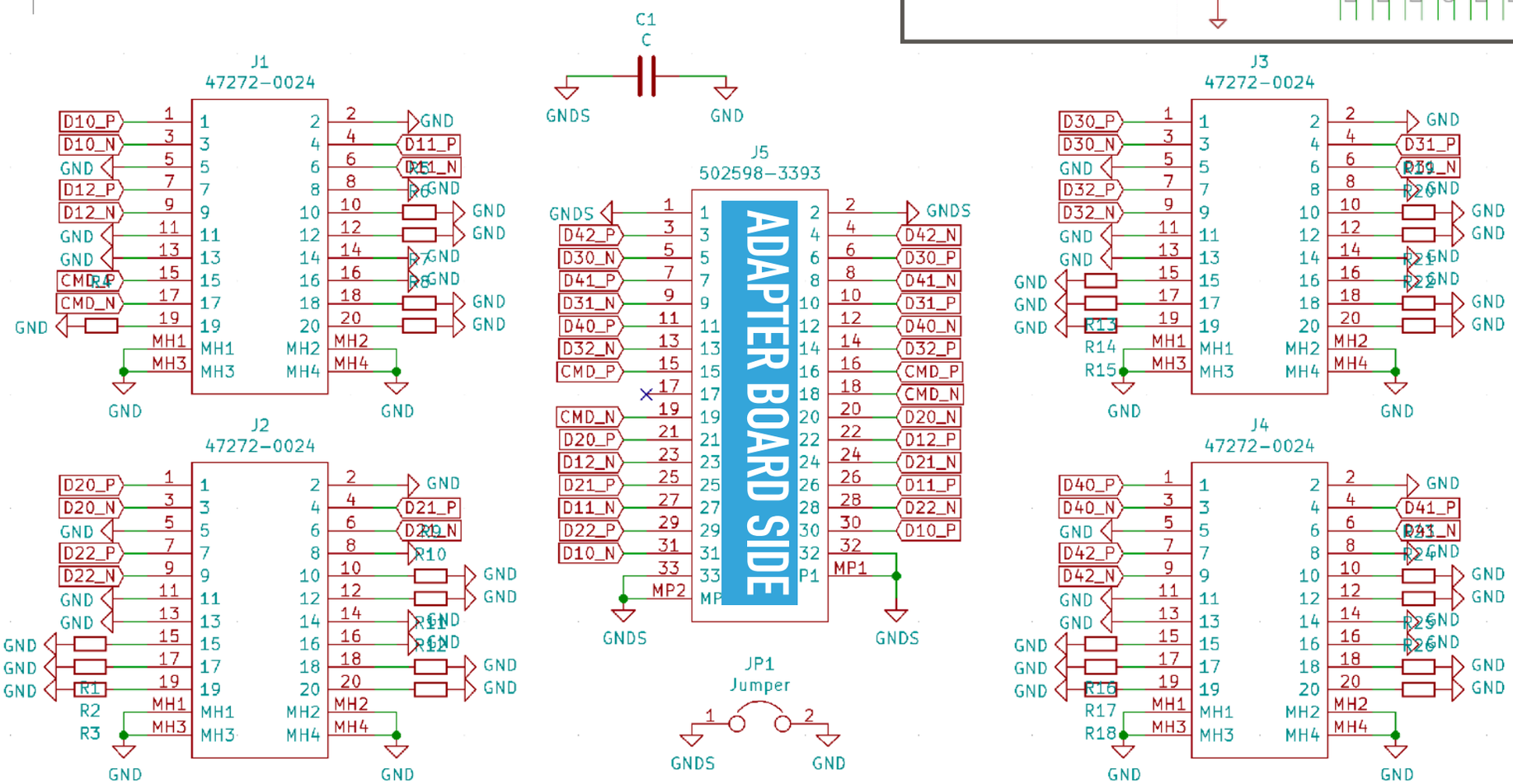
No Errors

```
 ---> Mask Stage 23
 ---> Mask Stage 24
 ---> Mask Stage 25
 ---> Mask Stage 26
 ---> Mask Stage 27
 ---> Mask Stage 28
 ---> Mask Stage 29
 ---> Mask Stage 30
 ---> Mask Stage 31
 ---> Mask Stage 32
 ---> Mask Stage 33
 ---> Mask Stage 34
 ---> Mask Stage 35
 ---> Mask Stage 36
 ---> Mask Stage 37
 ---> Mask Stage 38
 ---> Mask Stage 39
 ---> Mask Stage 40
 ---> Mask Stage 41
 ---> Mask Stage 42
 ---> Mask Stage 43
 ---> Mask Stage 44
 ---> Mask Stage 45
 ---> Mask Stage 46
 ---> Mask Stage 47
 ---> Mask Stage 48
 ---> Mask Stage 49
 ---> Mask Stage 50
 ---> Mask Stage 51
 ---> Mask Stage 52
 ---> Mask Stage 53
 ---> Mask Stage 54
 ---> Mask Stage 55
 ---> Mask Stage 56
 ---> Mask Stage 57
 ---> Mask Stage 58
 ---> Mask Stage 59
 ---> Mask Stage 60
 ---> Mask Stage 61
 ---> Mask Stage 62
 ---> Mask Stage 63
-> Scan done!
```

SCHEMATIC DIAGRAM







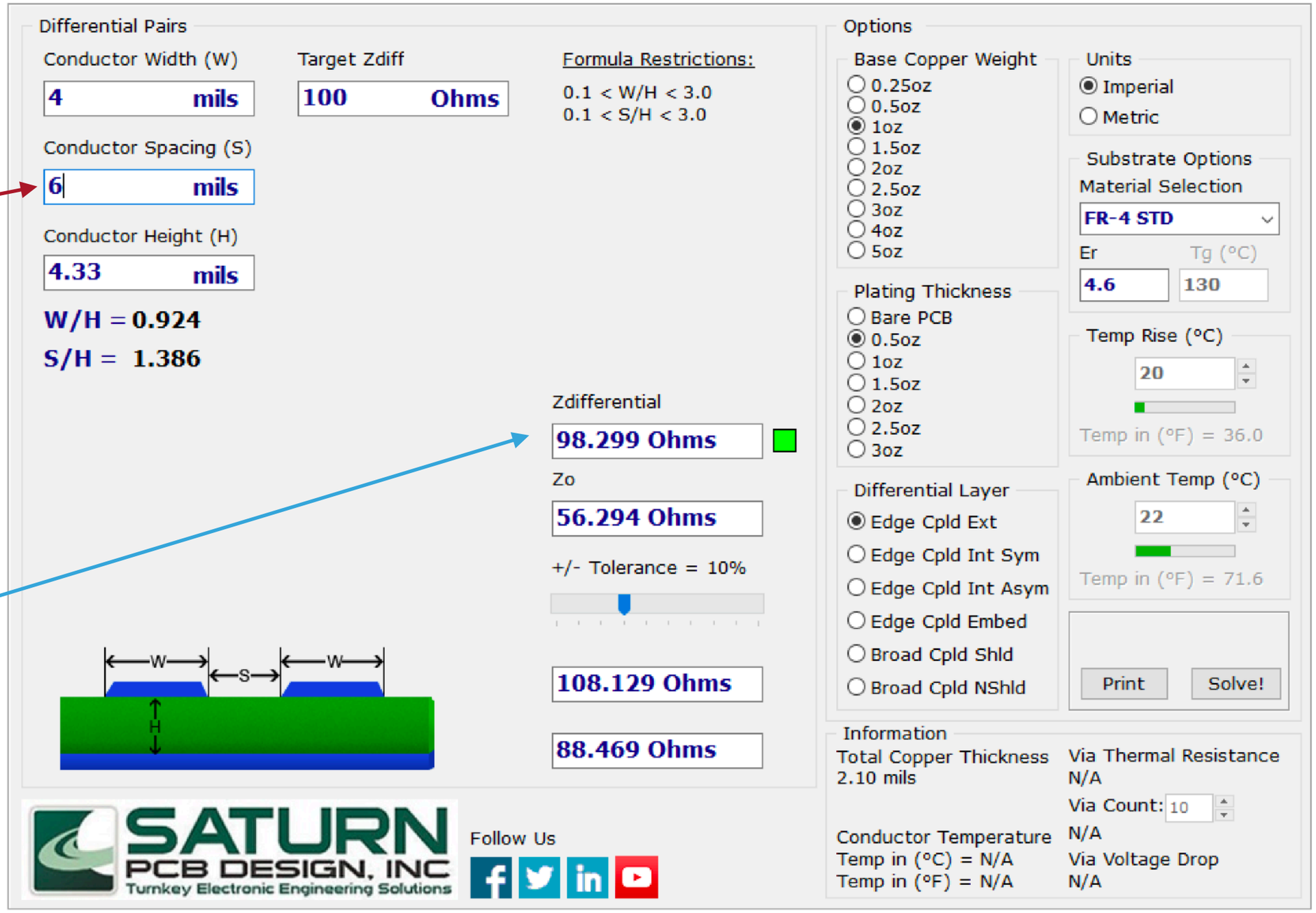
PIN ASSIGNMENT ACCORDING TO THE RD53 QUAD V3.6

LINE IMPEDANCE – CALCULATION

Changed this from 4 mil to 6 mil

Differential line impedance is ~ 100 Ω

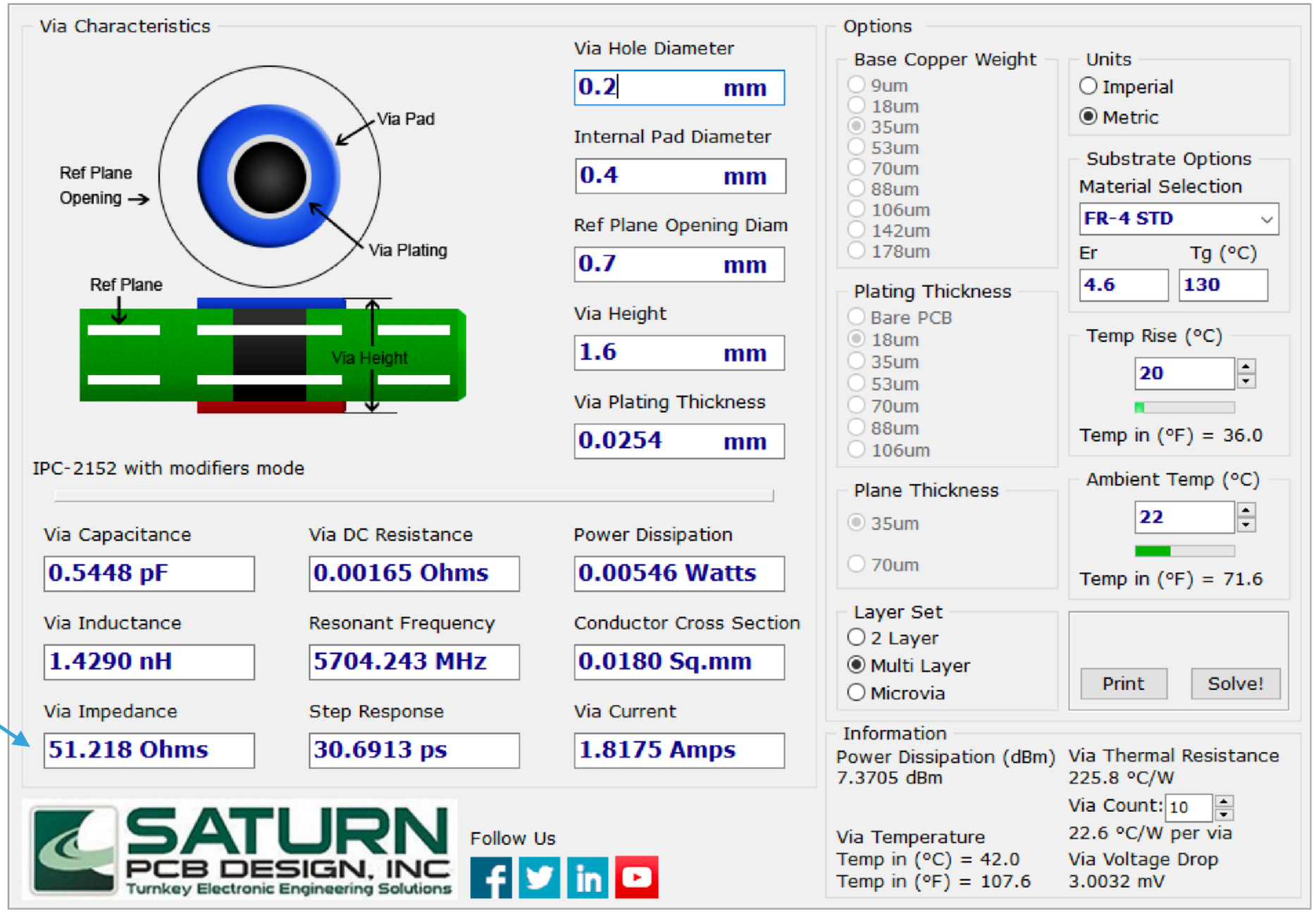
Single line impedance is ~ 50 Ω



VIA IMPEDANCE – CALCULATION

I didn't consider via impedance earlier

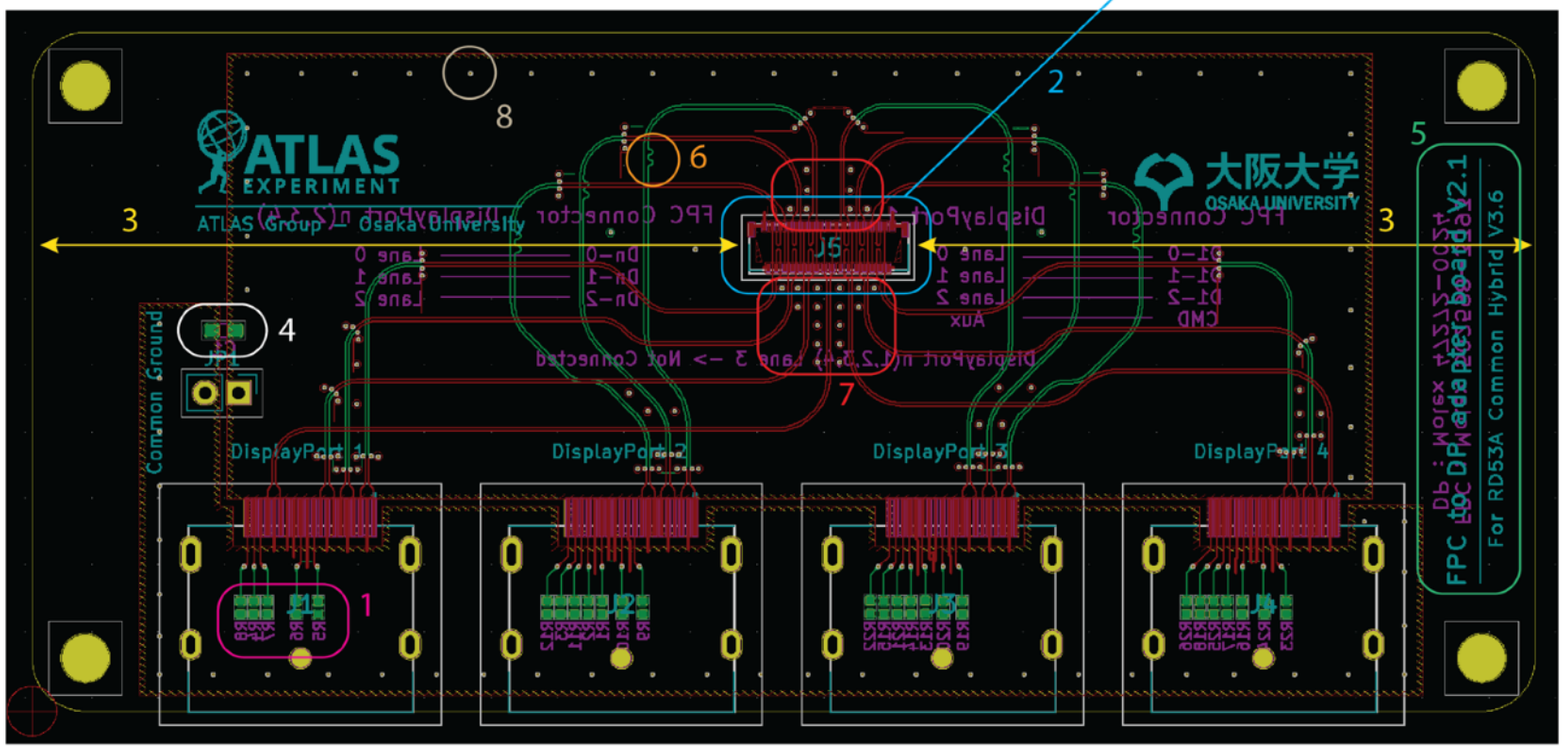
Single lane impedance is ~ 50 Ω



4 DISPLAY PORT ADAPTER CARD VERSION 2.1

Features

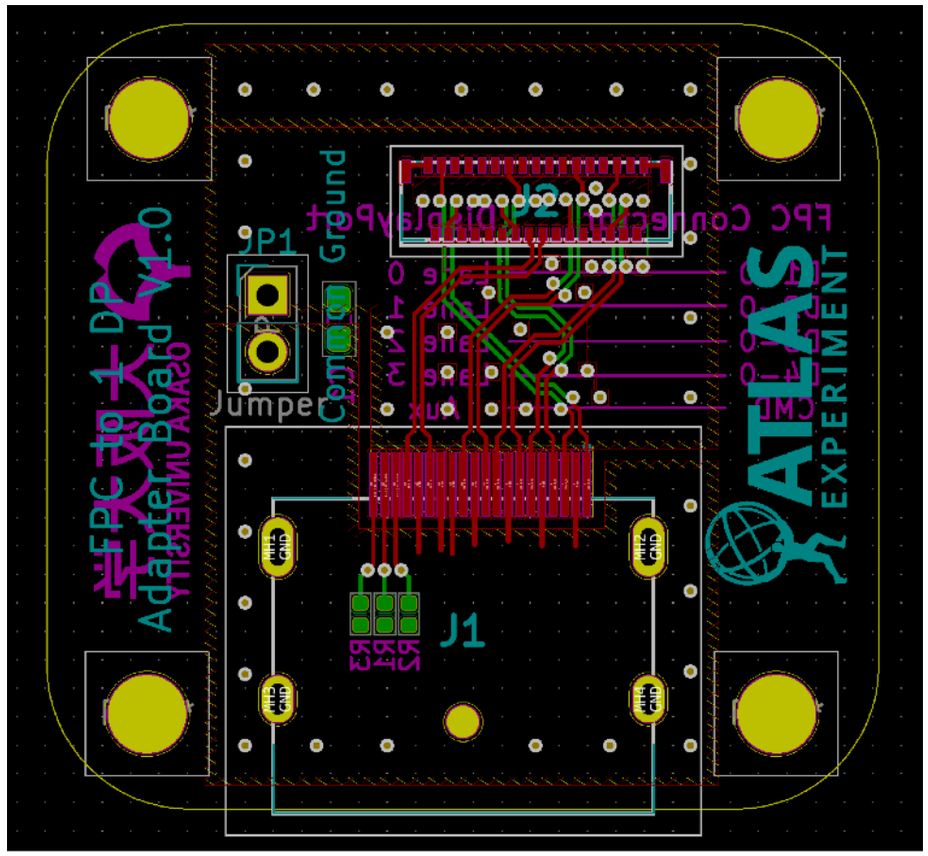
- All lines are same length in a 1 mm order.
- All lines are smooth, without any angled corners.
- All lines are adjusted to 100 ± 10 Ω Diff.Impedance.
- All vias are adjusted to 50 ± 5 Ω Impedance.



1. Added grounding resistors (50 Ω, so it looks 100 Ω in differential) to the floating lines.
2. Got rid of the vias, and added skewed lines (Referred to Ilya's RD53a Common Hybrid Design)
3. Shifted the FPC Connector a bit to the right. This way, the lines are more symmetric.
4. Added a capacitor (100 nF ?) so there is a AC coupled ground.
5. Added the version number to the front, and connector part number to the back.
6. The skew is adjusted with a few meanders, just after the point where the skew got shifted.
7. Added grounding vias next to Differential Lanes, to reduce cross-talk.
8. Added grounding vias around the board, to make signals less prone to noise from outside.

Updates compared to the previous version

1 DISPLAY PORT ADAPTER CARD VERSION 1.0

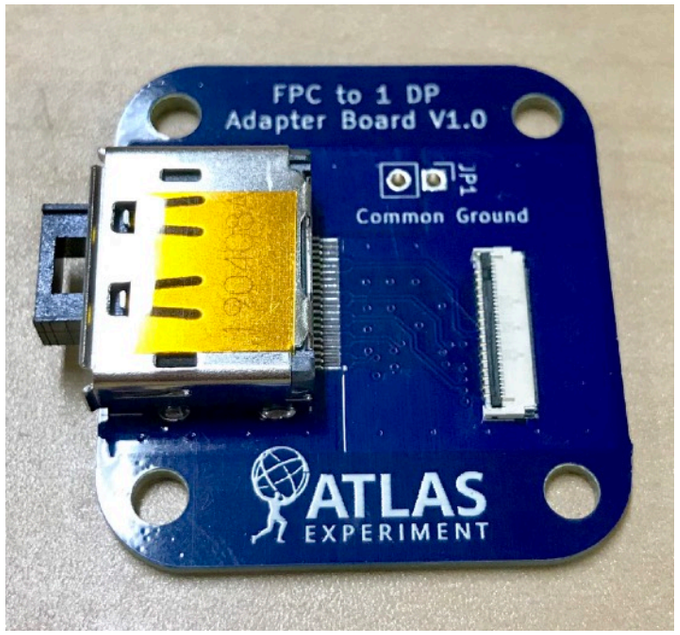


Similar changes as the previous slide were made !

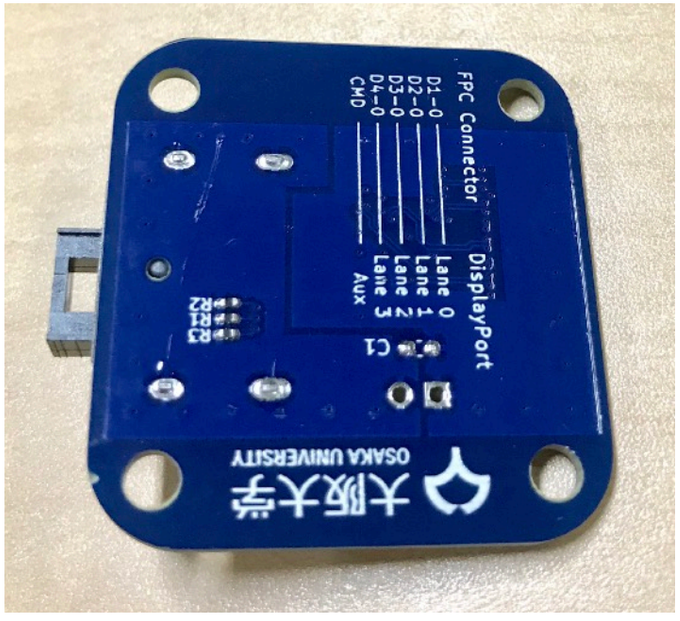
Features

- The skew is corrected
- All lines (except CMD) are of same length
- No meanders on the lines

Front

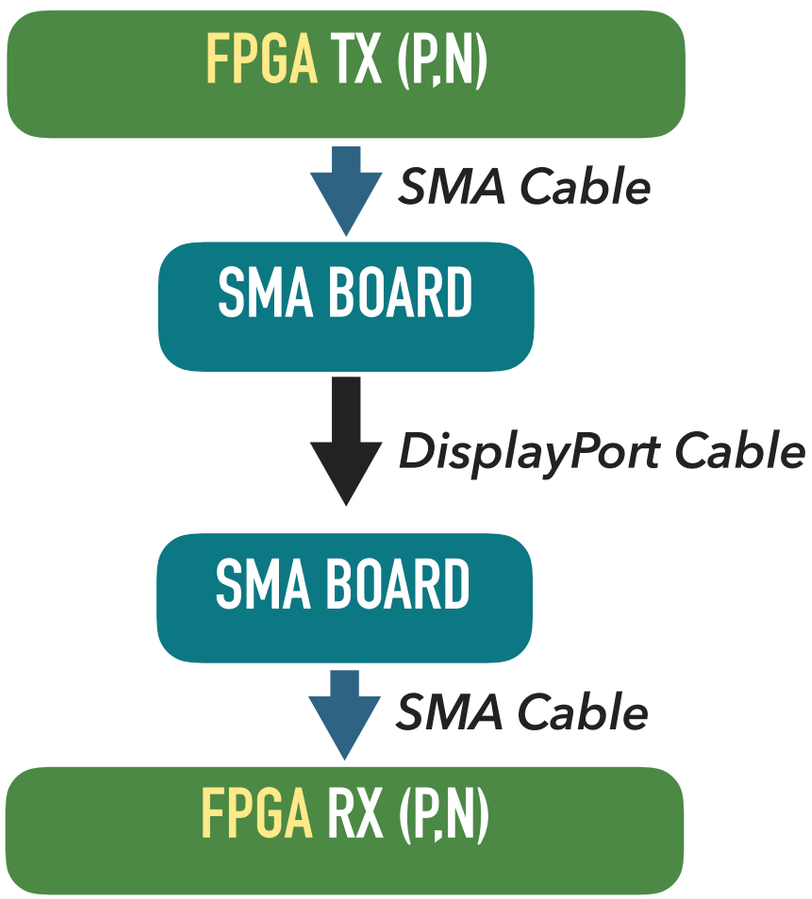


Back

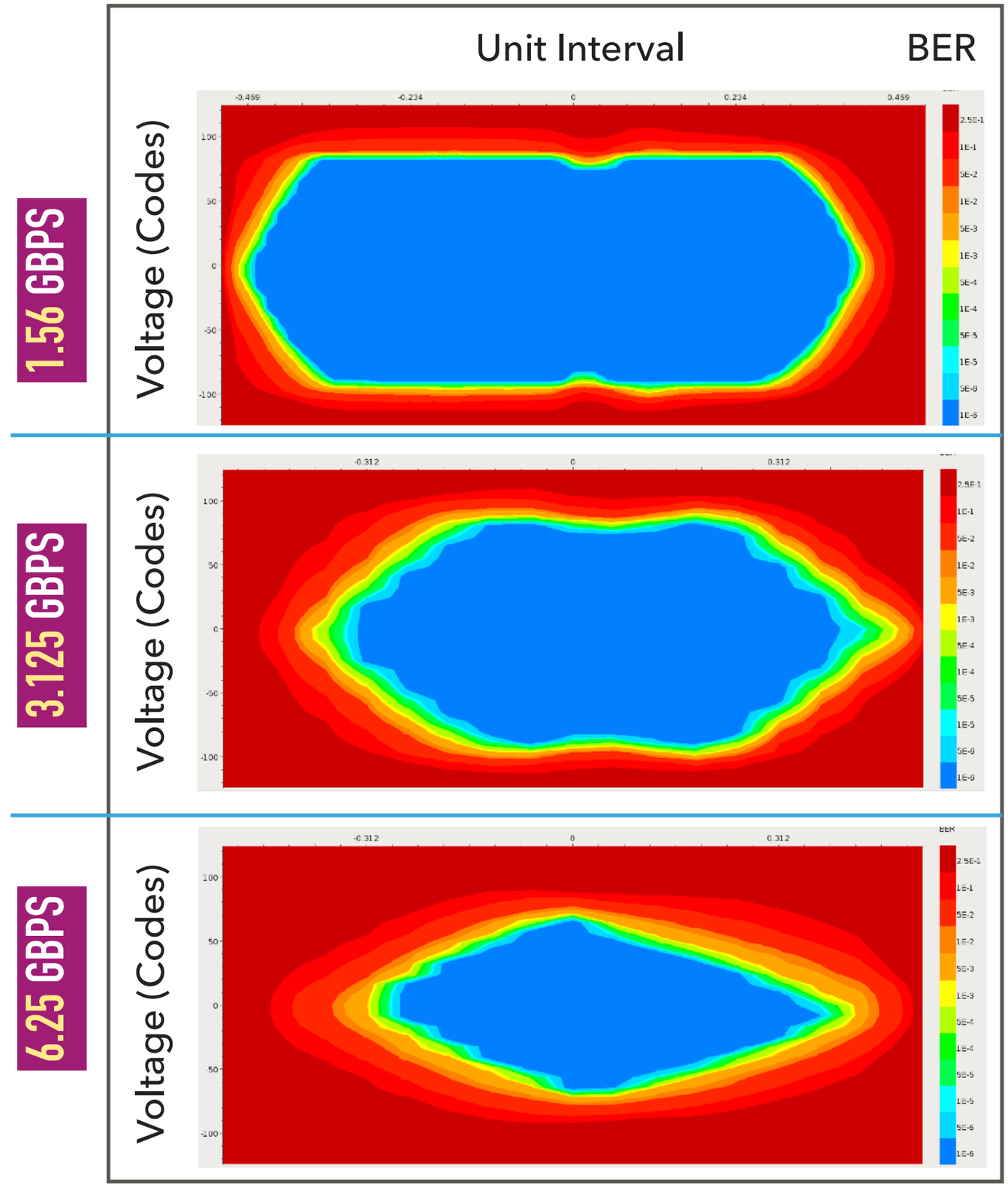


IBERT – STEP 1

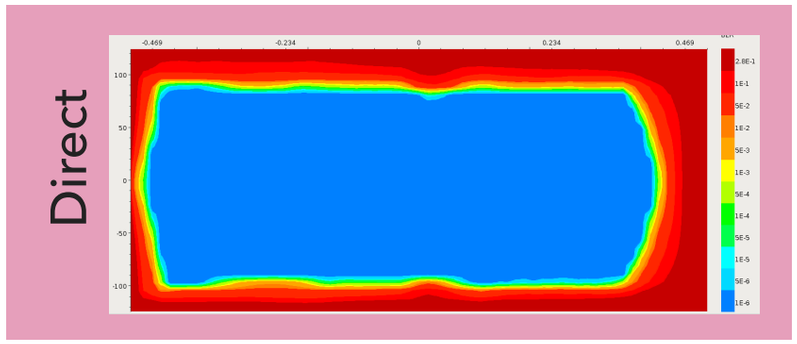
TX (P,N) to SMA to RX (P,N)

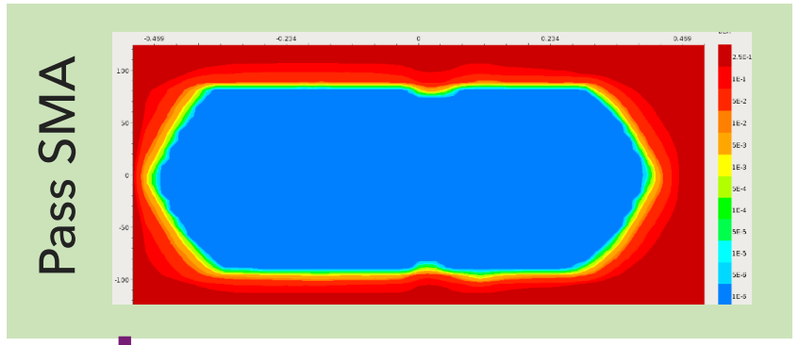


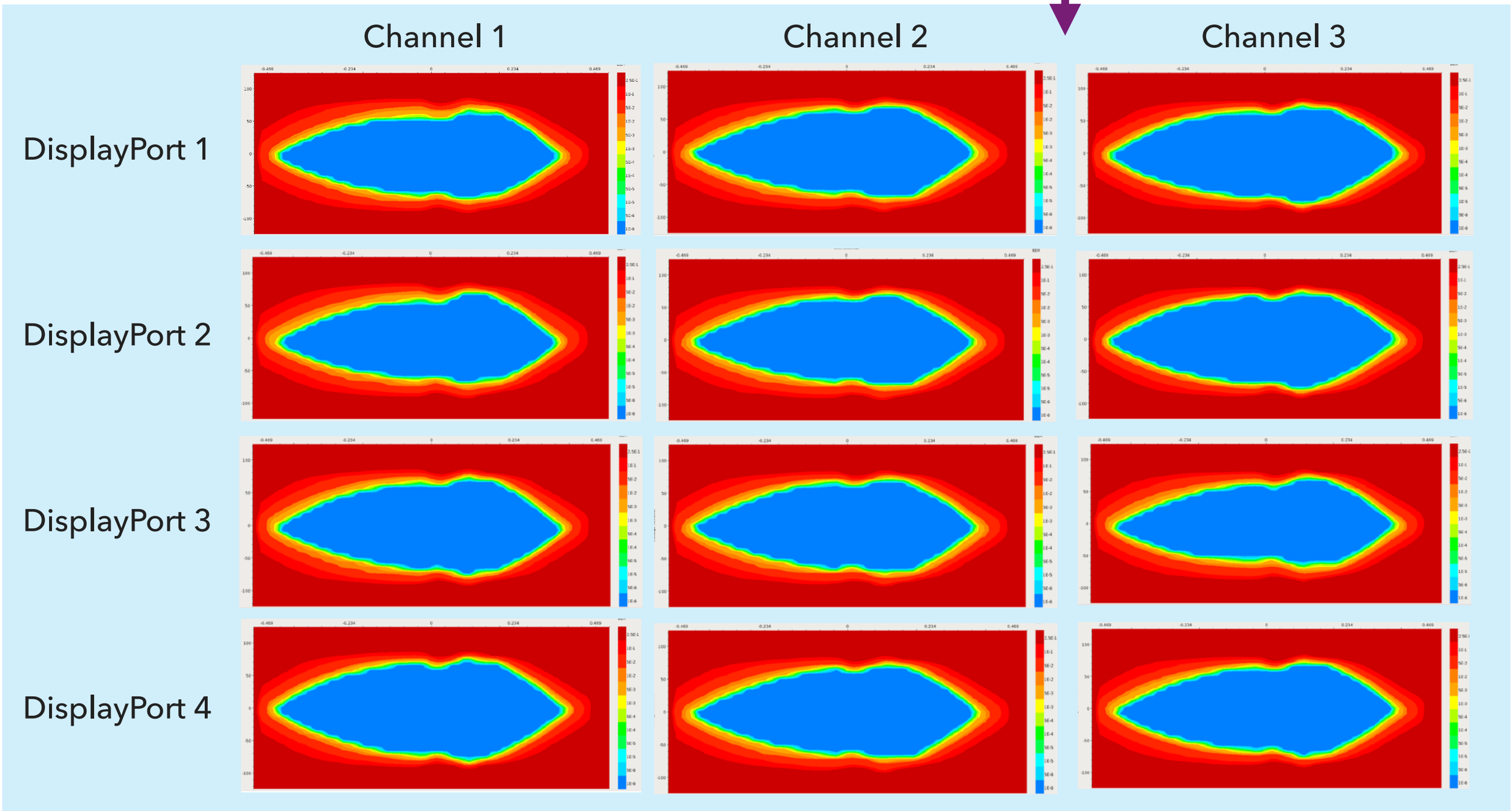
Please check backup slides for more details



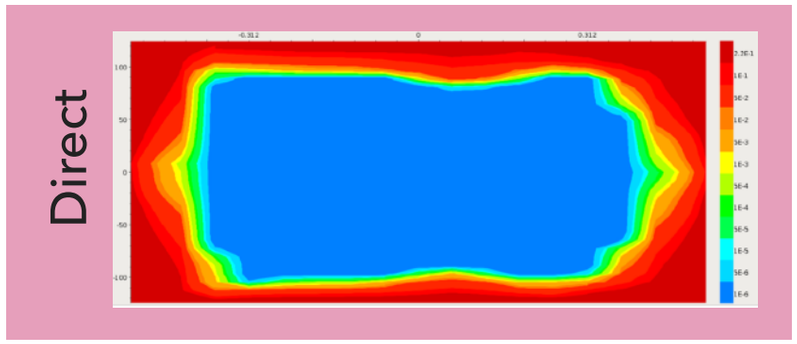
1.56 Gbps SCANS

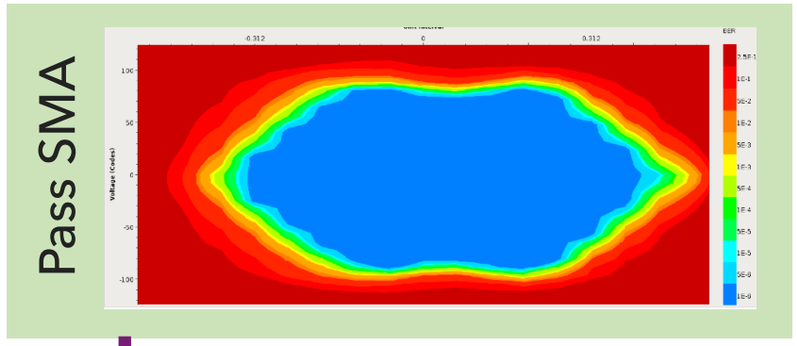


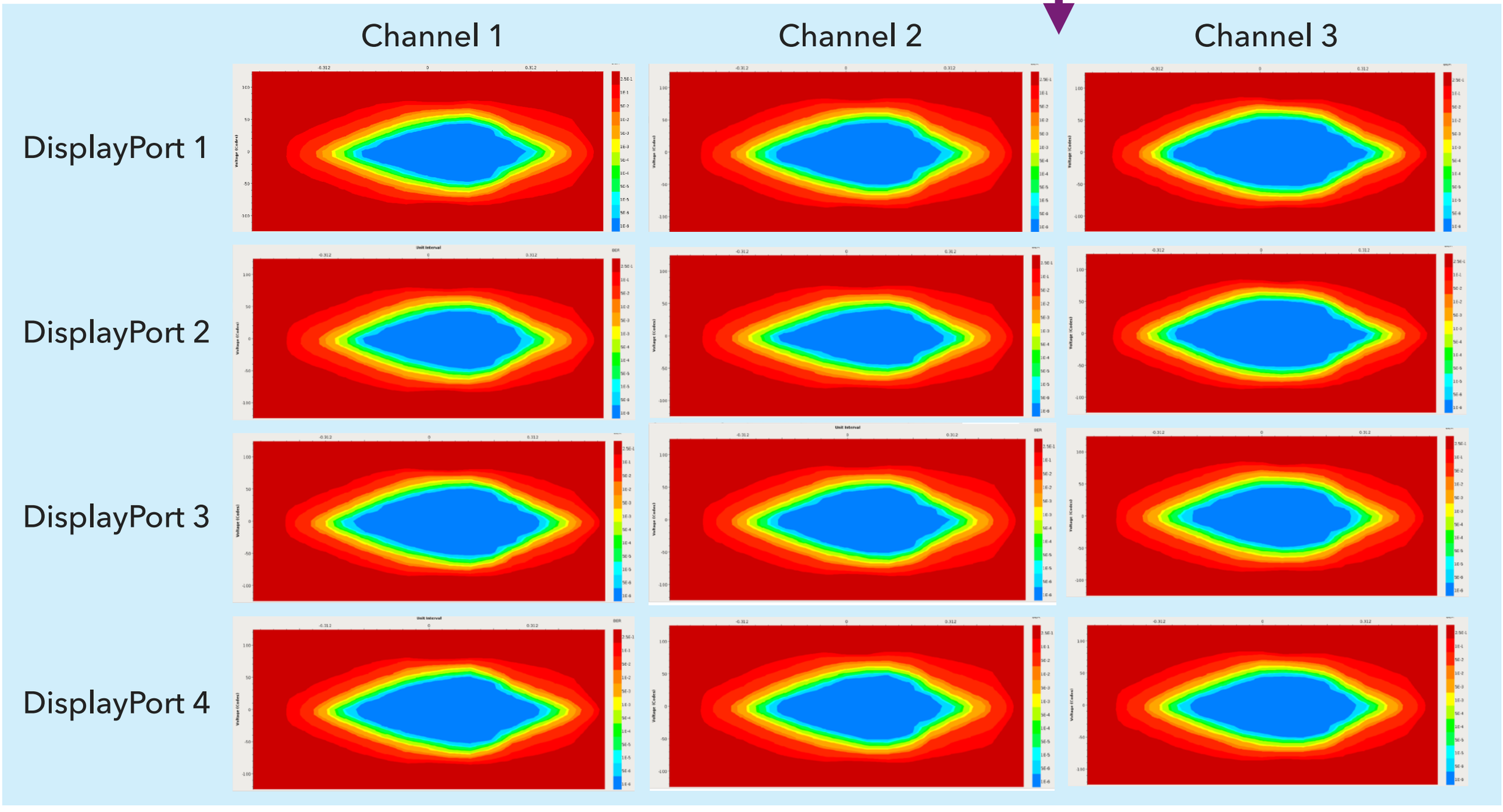




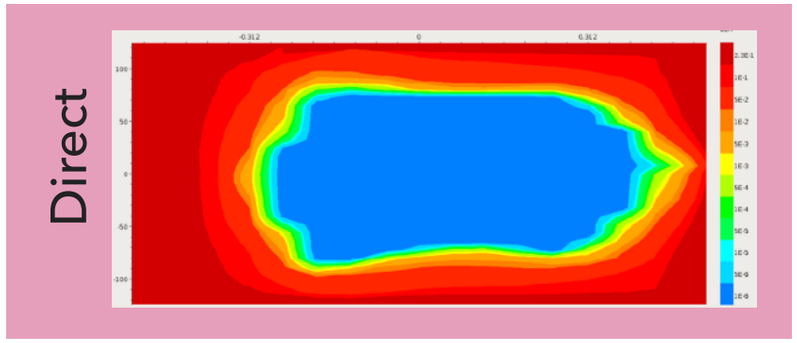
3.125 Gbps SCANS

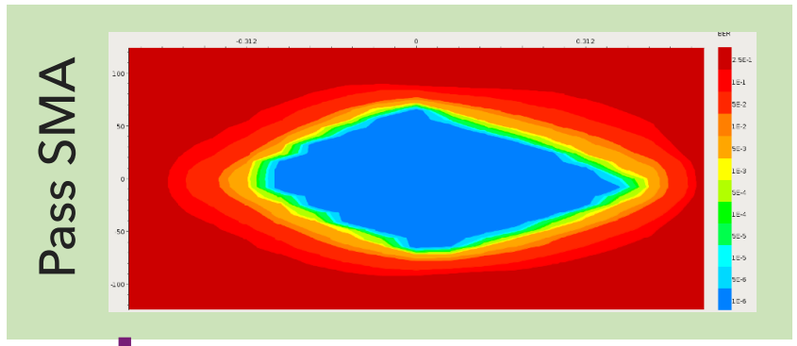


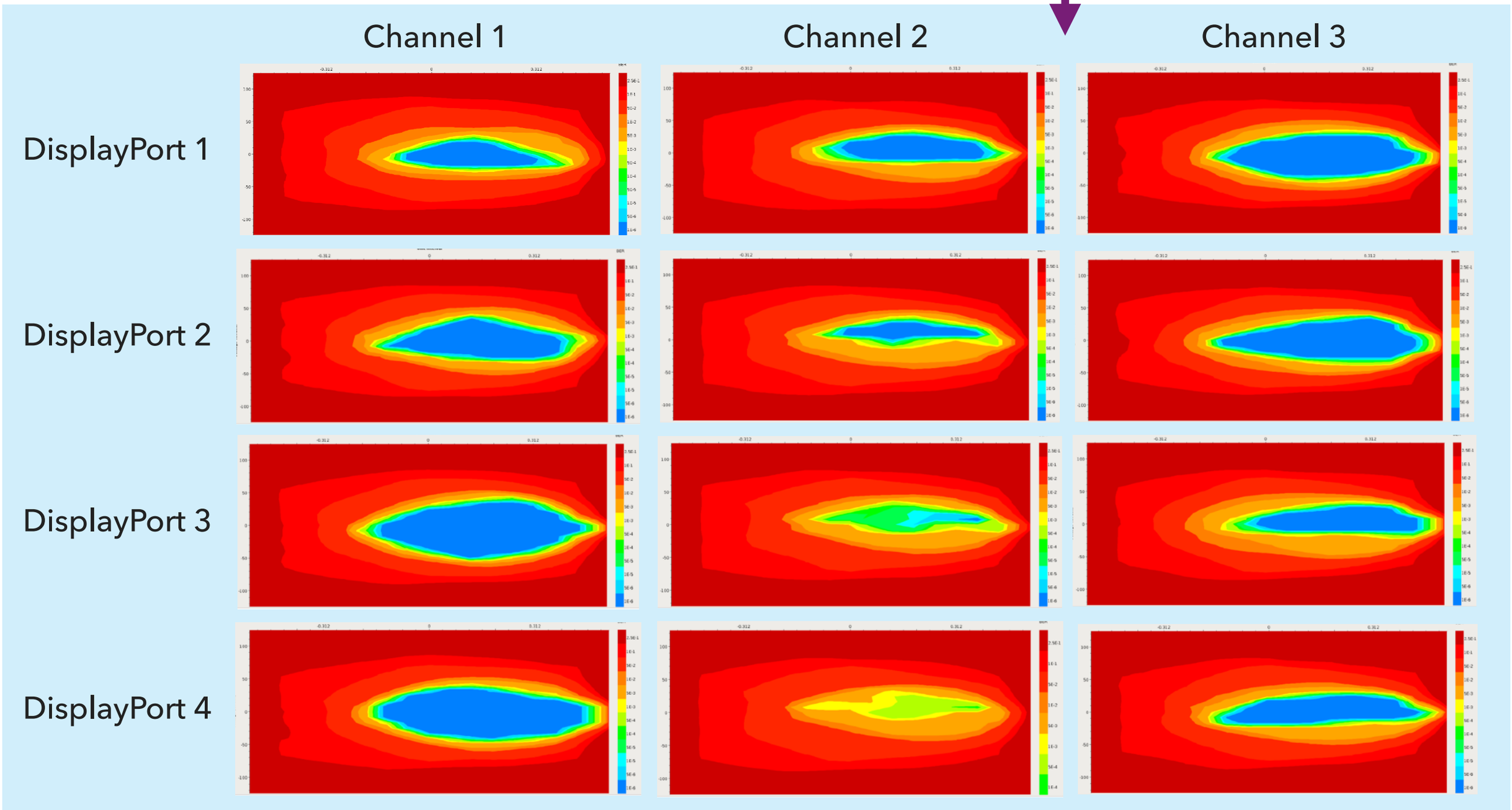




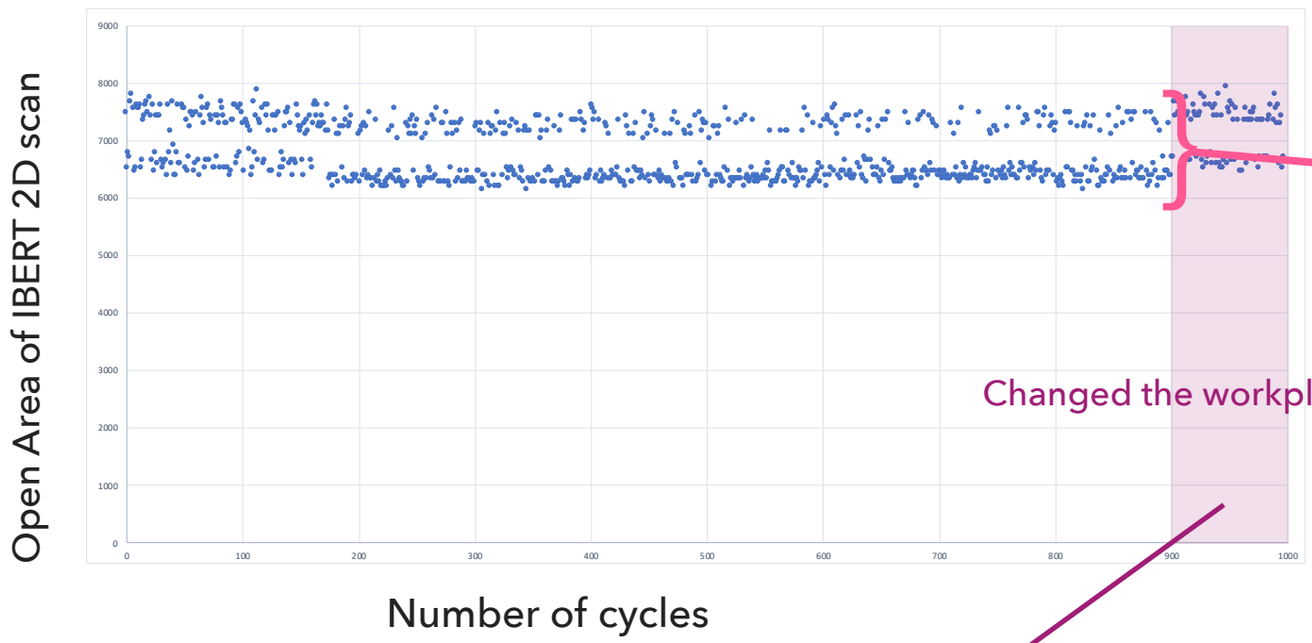
6.25 Gbps SCANS

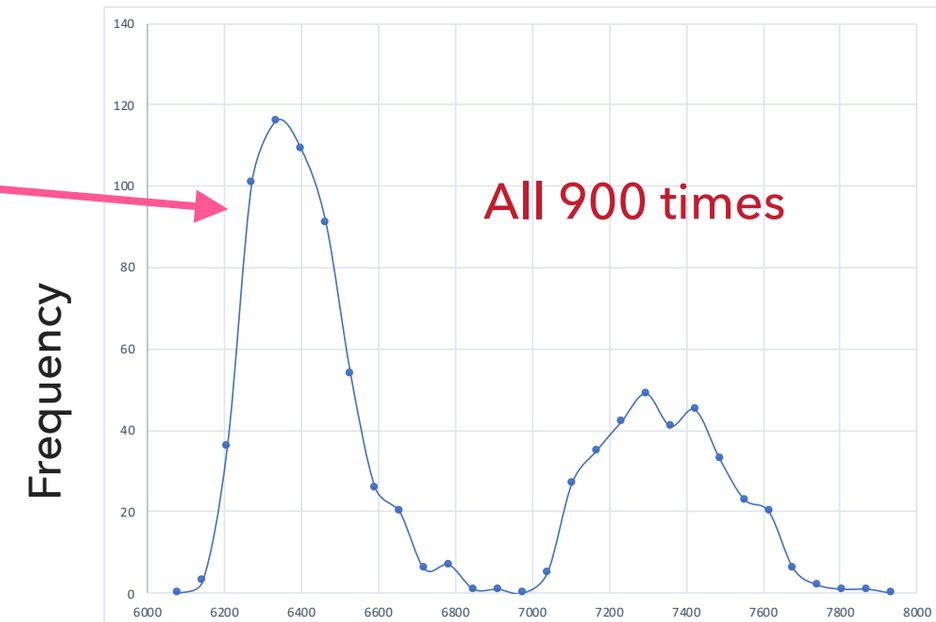


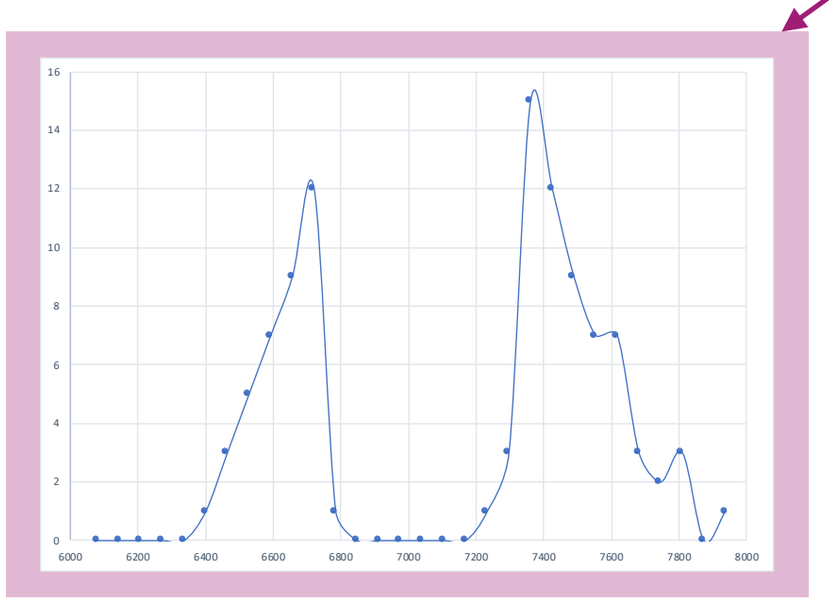




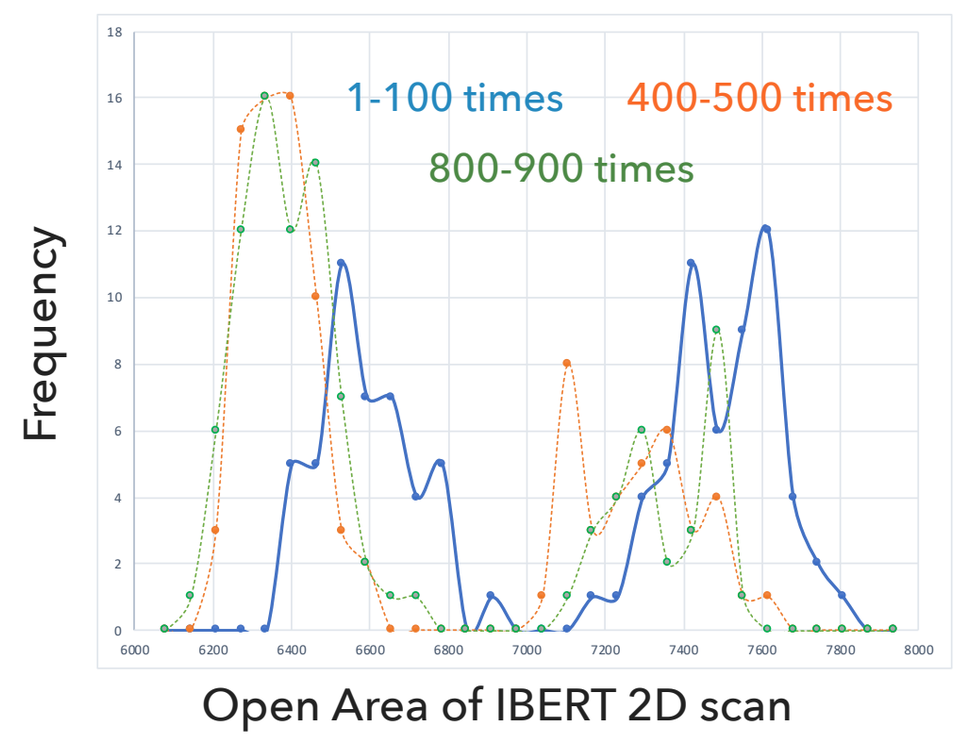
DURABILITY OF THE CONNECTOR – 1000 TIMES



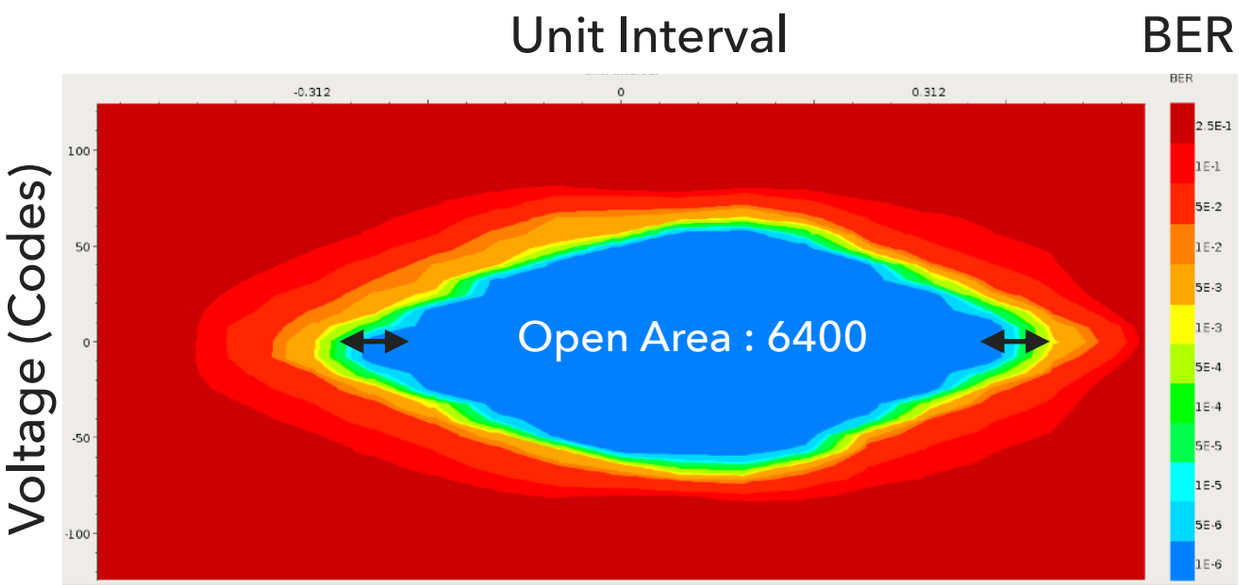




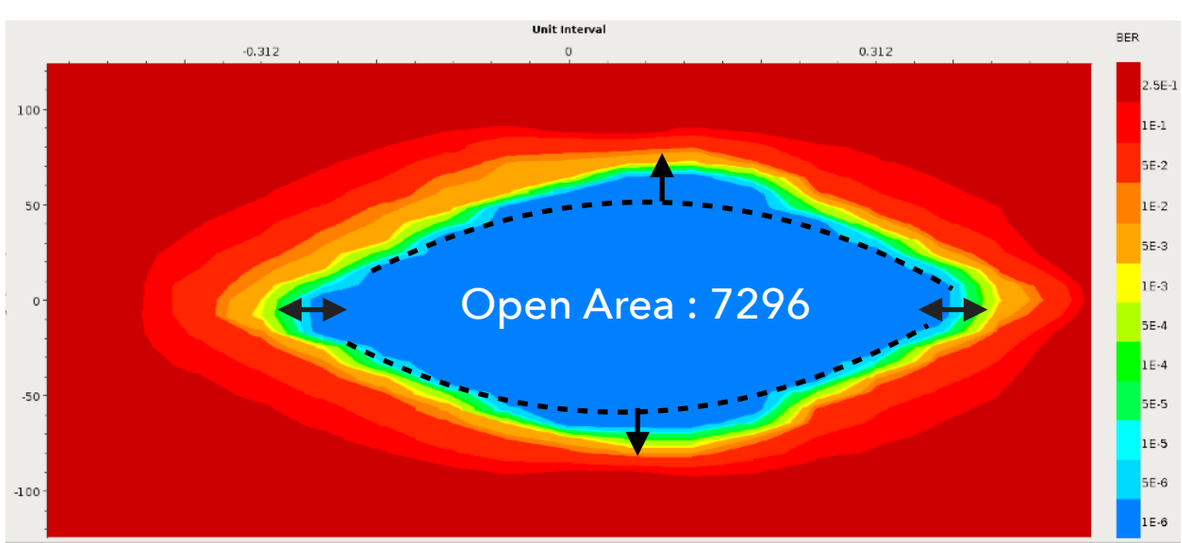
THE PROBABILITY OF >7000 HAS REDUCED, WITH INCREASING CYCLES.



REASON FOR THE SPLITTING – GUESS



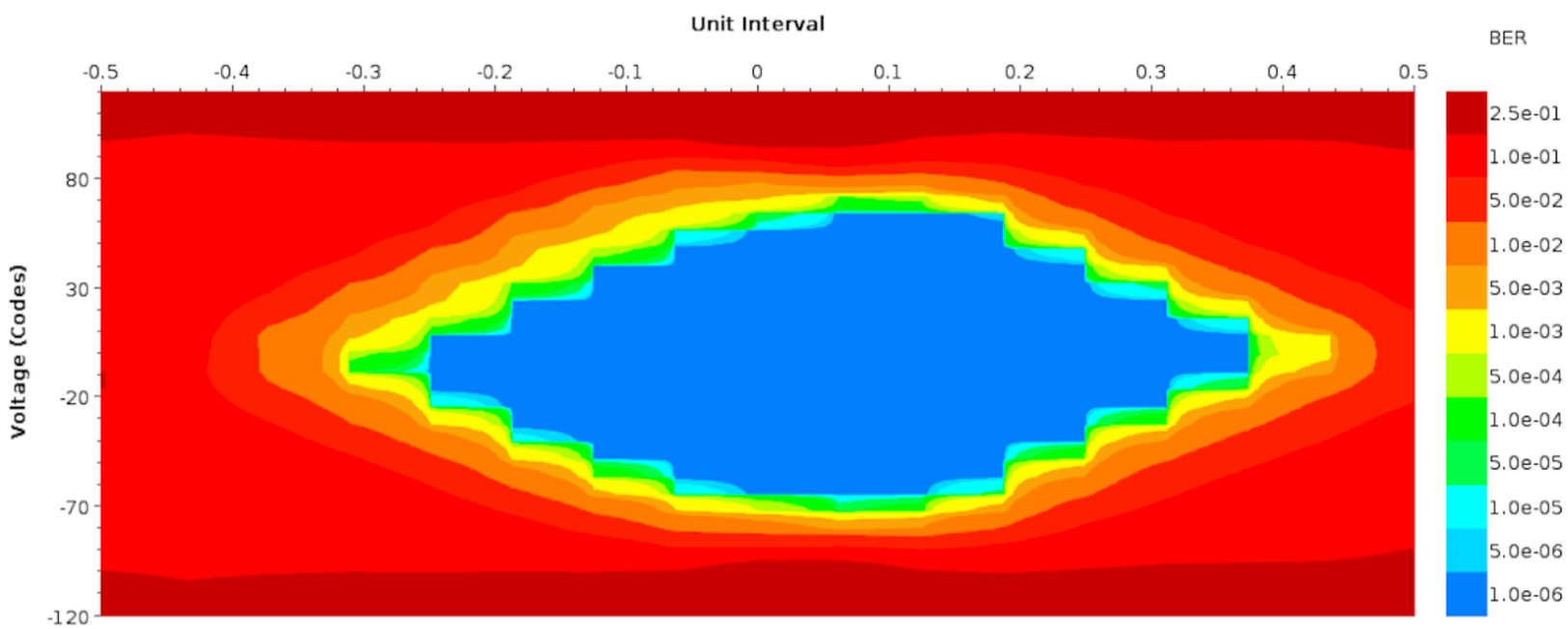
Horizontal Variation - More Continuous



Vertical Variation - More Discrete

MEANING OF THE AREA

- Vertical Increment : 8, Horizontal Increment : 8
- Unit increment in area : 64



Summary	
Name:	SCAN_10
Description:	Scan 10
Started:	2019-Oct-01 14:33:50
Ended:	2019-Oct-01 14:33:53

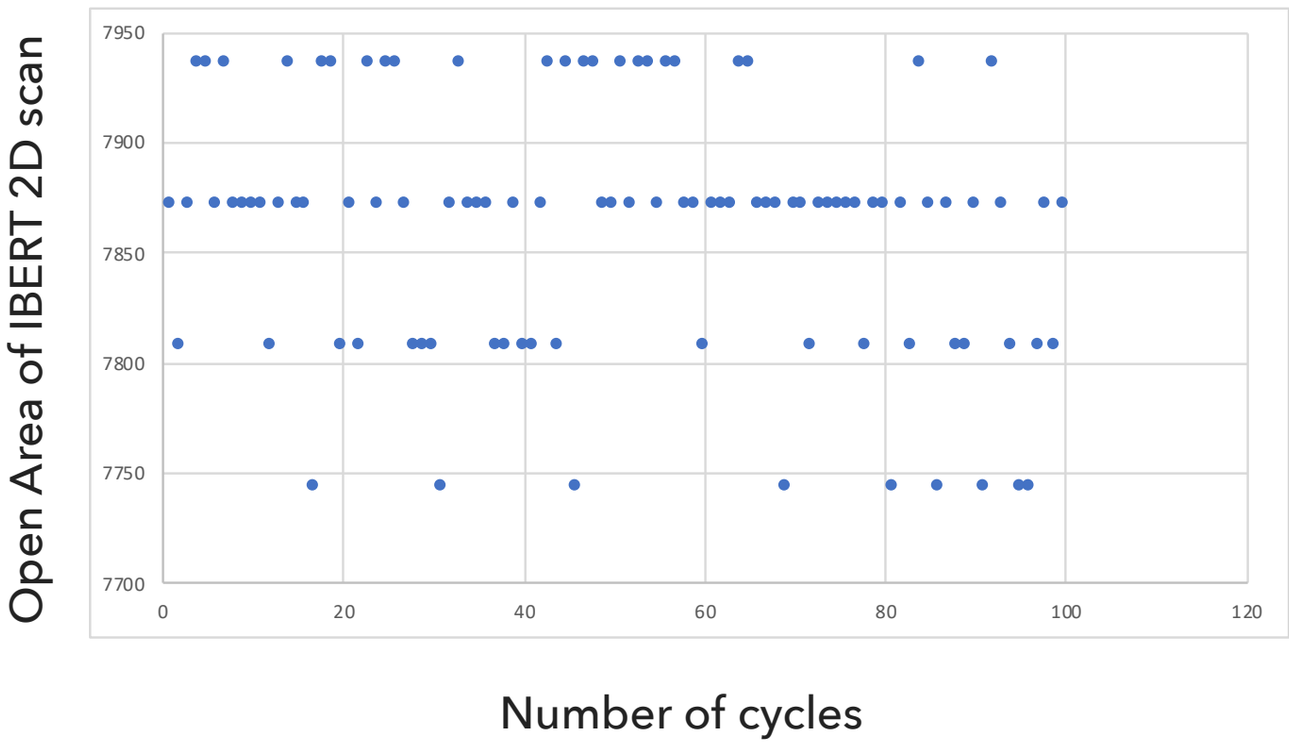
Metrics	
Open area:	7872
Open UI %:	64.71

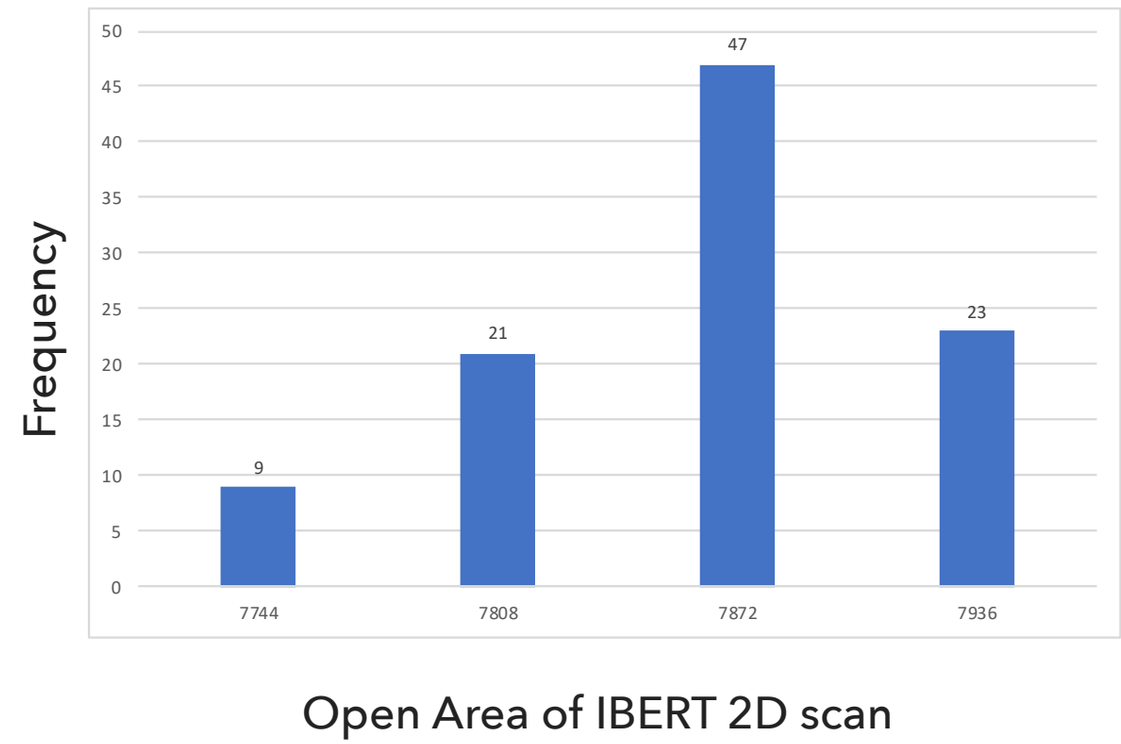
Settings	
Link settings:	N/A
Horizontal increment:	8
Horizontal range:	-0.500 UI to 0.500 UI
Vertical increment:	8
Vertical range:	100%

The horizontal axis increases in 8 units & the vertical axis increases in 8 units

IBERT OPEN AREA VARIATION – 100 TIMES

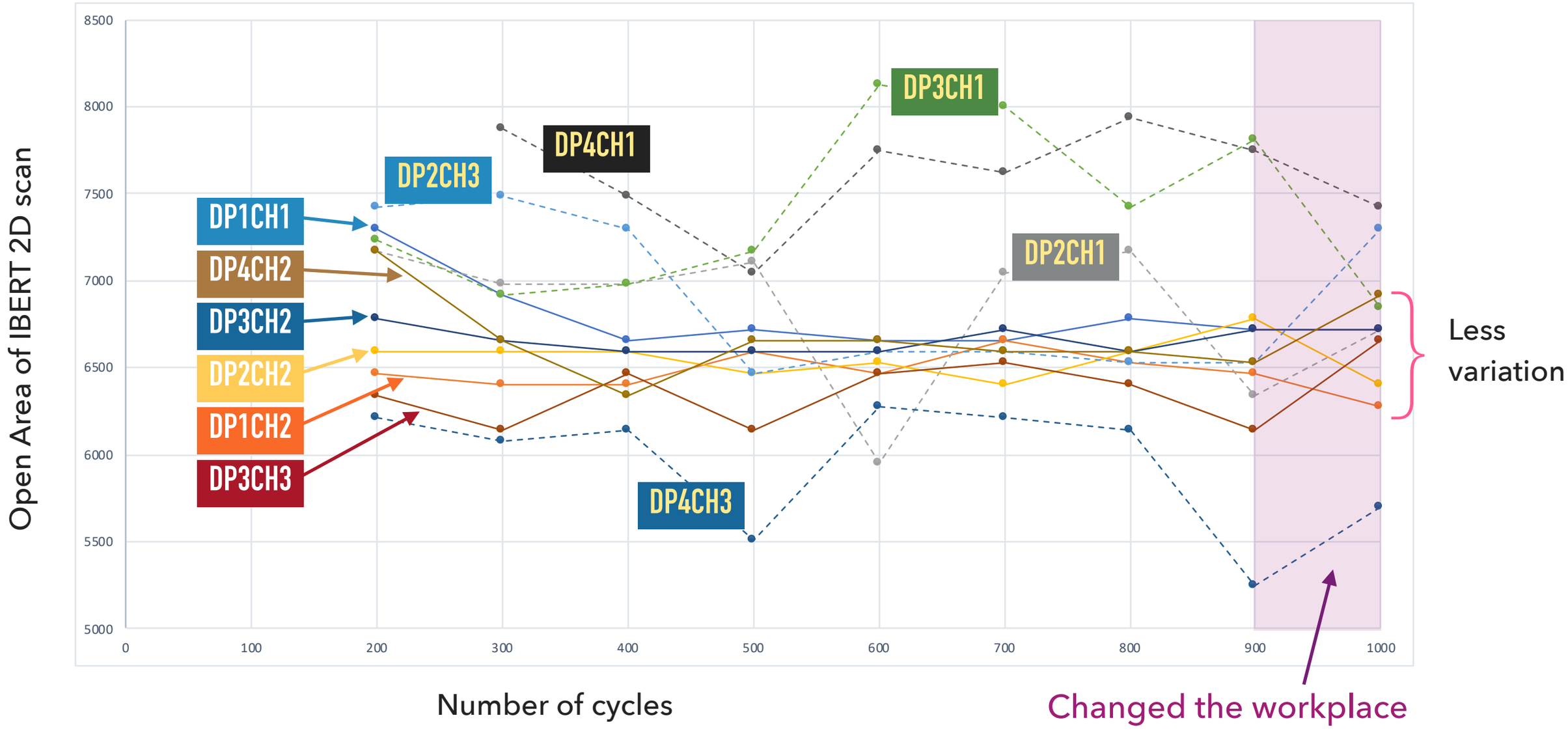
- Without connecting/disconnecting (DP1Ch3)





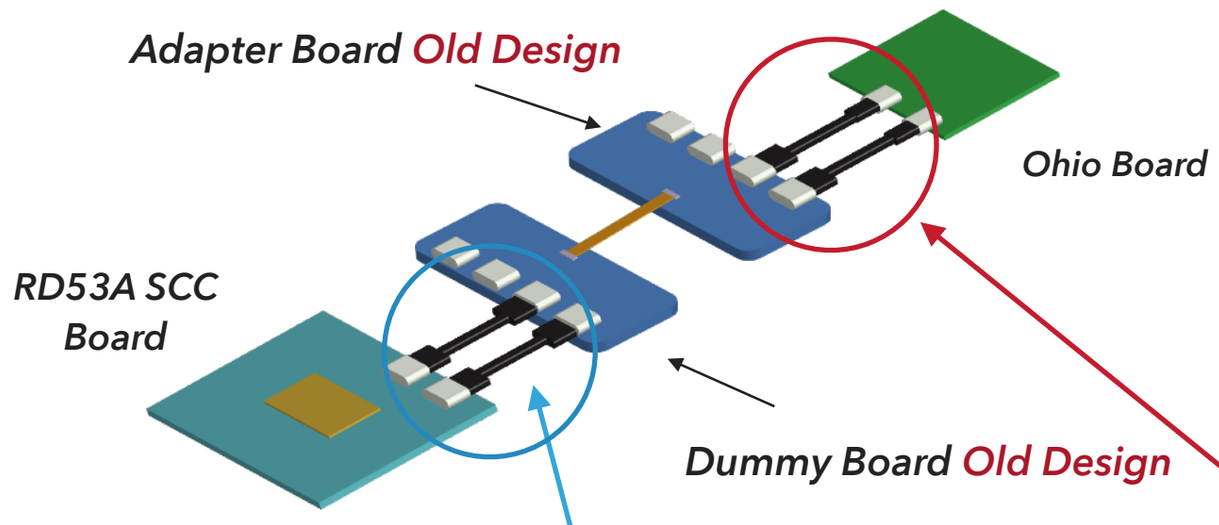
For every reading there is a variation. This should be taken into consideration.

OTHER CHANNELS – 1000 TIMES



- Dashed line channels show a big variation compared to solid line channels.

CURRENT SET-UP



DisplayPort ➡ DisplayPort Cable

Receptacle On Source Device			DisplayPort Standard Cable						Receptacle on the Sink Device		
			Source Side Plug			Cable Wiring	Sink Side Plug				
At SOURCE		Pin#	At SOURCE		Pin#		Pin#	At SINK		Pin#	Sink End Dongle	
Signal Type			Signal Type					Signal Type			Signal Type	
Out	ML_Lane 0(p)	1	Out	ML_Lane 0(p)	1		1	ML_Lane 3 (n)	In	1	ML_Lane 3 (n)	In
GND	GND	2	GND	GND	2		2	GND	GND	2	GND	GND
Out	ML_Lane 0 (n)	3	Out	ML_Lane 0 (n)	3		3	ML_Lane 3 (p)	In	3	ML_Lane 3 (p)	In
Out	ML_Lane 1 (p)	4	Out	ML_Lane 1 (p)	4		4	ML_Lane 2 (n)	In	4	ML_Lane 2 (n)	In
GND	GND	5	GND	GND	5		5	GND	GND	5	GND	GND
Out	ML_Lane 1 (n)	6	Out	ML_Lane 1 (n)	6		6	ML_Lane 2 (p)	In	6	ML_Lane 2 (p)	In
Out	ML_Lane 2 (p)	7	Out	ML_Lane 2 (p)	7		7	ML_Lane 1 (n)	In	7	ML_Lane 1 (n)	In
GND	GND	8	GND	GND	8		8	GND	GND	8	GND	GND
Out	ML_Lane 2 (n)	9	Out	ML_Lane 2 (n)	9		9	ML_Lane 1 (p)	In	9	ML_Lane 1 (p)	In
Out	ML_Lane 3 (p)	10	Out	ML_Lane 3 (p)	10		10	ML_Lane 0 (n)	In	10	ML_Lane 0 (n)	In
GND	GND	11	GND	GND	11		11	GND	GND	11	GND	GND
Out	ML_Lane 3 (n)	12	Out	ML_Lane 3 (n)	12		12	ML_Lane 0 (p)	In	12	ML_Lane 0 (p)	In
CONFIG	CONFIG1	13	CONFIG	CONFIG1	13		13	CONFIG1	CONFIG	13	CONFIG1	CONFIG
CONFIG	CONFIG2	14	CONFIG	CONFIG2	14		14	CONFIG2	CONFIG	14	CONFIG2	CONFIG
I/O	AUX_CH (p)	15	I/O	AUX_CH (p)	15		15	AUX_CH (p)	I/O	15	AUX_CH (p)	I/O
GND	GND	16	GND	GND	16		16	GND	GND	16	GND	GND
I/O	AUX_CH (n)	17	I/O	AUX_CH (n)	17		17	AUX_CH (n)	I/O	17	AUX_CH (n)	I/O
In	Hot Plug Detect	18	In	Hot Plug Detect	18		18	Hot Plug Detect	Out	18	Hot Plug Detect	Out
PWR RTN	Return DP_PWR	19		Return DP_PWR	19		19	Return DP_PWR		19	Return DP_PWR	PWR RTN
PWR Out	DP_PWR	20		DP_PWR	20		20	DP_PWR		20	DP_PWR	PWR Out

SMT Solder Tail Side

SMT Solder tails Side

DisplayPort ➡ Mini DisplayPort Cable

DisplayPort Source Connector			DisplayPort to Mini DP Cable Assembly			Mini DP Sink Connector		
Signal Type	Pin Name	Pin	Plug Pin		Plug Pin	Pin	Pin Name	Signal Type
GND	GND	2	2	⟷	8	8	GND	GND
Out	ML_Lane 0 (p)	1	1	⟷	12	12	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	3	3	⟷	10	10	ML_Lane 0 (n)	In
GND	GND	5	5	⟷	13	13	GND	GND
Out	ML_Lane 1 (p)	4	4	⟷	17	17	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	6	6	⟷	15	15	ML_Lane 1 (n)	In
GND	GND	8	8	⟷	7	7	GND	GND
Out	ML_Lane 2 (p)	7	7	⟷	11	11	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	9	9	⟷	9	9	ML_Lane 2 (n)	In
GND	GND	19	19	⟷	19	19	GND	GND
In	Hot Plug Detect	18	18	⟷	2	2	Hot Plug Detect	Out
CFG	CONFIG1	13	13	⟷	4	4	CONFIG1	CFG
CFG	CONFIG2	14	14	⟷	6	6	CONFIG2	CFG
GND	GND	11	11	⟷	1	1	GND	GND
Out	ML_Lane 3 (p)	10	10	⟷	5	5	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12	12	⟷	3	3	ML_Lane 3 (n)	In
GND	GND	16	16	⟷	14	14	GND	GND
I/O	AUX_CH (p)	15	15	⟷	16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	17	17	⟷	18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20	20	(no connection)	20	20	DP_PWR	PWR Out

Figure 2-10: DisplayPort to Mini DisplayPort Cable Connector Assembly Wiring

MANAGED TO SOLVE THE READOUT PROBLEM

ASIC		FPGA
Lane		Lane
CMD P	↔	CMD P
CMD N	↔	CMD N
GTX 3 P	↔	GTX 0 N
GTX 3 N	↔	GTX 0 P
GTX 2 P	↔	GTX 1 N
GTX 2 N	↔	GTX 1 P
GTX 1 P	↔	GTX 2 N
GTX 1 N	↔	GTX 2 P
GTX 0 P	↔	GTX 3 N
GTX 0 N	↔	GTX 3 P

Made a new constraint file, and edited to this configuration

```
bram_fei4_octa_lbnl            constrs_kc705_dual_lakmin_dummy.xdc
bram_fei4_single_osaka         constrs_kc705_dual_ohio.xdc
bram_rd53a_octa_ohio           constrs_kc705_fmccard-fei4b-osaka.xdc
bram_rd53a_quad_ohio           constrs_kc705_timing.xdc
bram_rd53a_quad_osaka_dummy    constrs_kc705_vhdci-fei4-rj45-adapter.xdc
bram_yarr_kc705.vhd            convert_xpressk7toKC705.sh
constrs_kc705.xdc
```

ASIC	SCC DP Connector		SCC DP Plug		Dummy DP Plug		Dummy DP Connector		Adapter DP Connector		Adapter DP Plug		Ohio Mini DP Plug		Ohio Mini DP Connector		FPGA
Lane	Pin	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Lane
CMD P	17	CMD N	17	CMD N	17	CMD N	17	CMD N	17	CMD N	17	CMD N	18	CMD N	18	CMD N	CMD P
CMD N	15	CMD P	15	CMD P	15	CMD P	15	CMD P	15	CMD P	15	CMD P	16	CMD P	16	CMD P	CMD N
GTX 3 P	12	GTX 3 N	12	GTX 3 N	1	GTX 0 P	1	GTX 0 P	1	GTX 0 P	1	GTX 0 P	12	GTX 0 P	12	GTX 0 P	GTX 0 N
GTX 3 N	10	GTX 3 P	10	GTX 3 P	3	GTX 0 N	3	GTX 0 N	3	GTX 0 N	3	GTX 0 N	10	GTX 0 N	10	GTX 0 N	GTX 0 P
GTX 2 P	9	GTX 2 N	9	GTX 2 N	4	GTX 1 P	4	GTX 1 P	4	GTX 1 P	4	GTX 1 P	17	GTX 1 P	17	GTX 1 P	GTX 1 N
GTX 2 N	7	GTX 2 P	7	GTX 2 P	6	GTX 1 N	6	GTX 1 N	6	GTX 1 N	6	GTX 1 N	15	GTX 1 N	15	GTX 1 N	GTX 1 P
GTX 1 P	6	GTX 1 N	6	GTX 1 N	7	GTX 2 P	7	GTX 2 P	7	GTX 2 P	7	GTX 2 P	11	GTX 2 P	11	GTX 2 P	GTX 2 N
GTX 1 N	4	GTX 1 P	4	GTX 1 P	9	GTX 2 N	9	GTX 2 N	9	GTX 2 N	9	GTX 2 N	9	GTX 2 N	9	GTX 2 N	GTX 2 P
GTX 0 P	3	GTX 0 N	3	GTX 0 N	10	GTX 3 P	10	GTX 3 P	10	GTX 3 P	10	GTX 3 P	5	GTX 3 P	5	GTX 3 P	GTX 3 N
GTX 0 N	1	GTX 0 P	1	GTX 0 P	12	GTX 3 N	12	GTX 3 N	12	GTX 3 N	12	GTX 3 N	3	GTX 3 N	3	GTX 3 N	GTX 3 P
	Source Side Pins		DisplayPort to DisplayPort Cable				Source Side Pins		Source Side Pins		DisplayPort to Mini-DisplayPort Cable				Sink Side Pins		

Compare the Green and Blue Columns

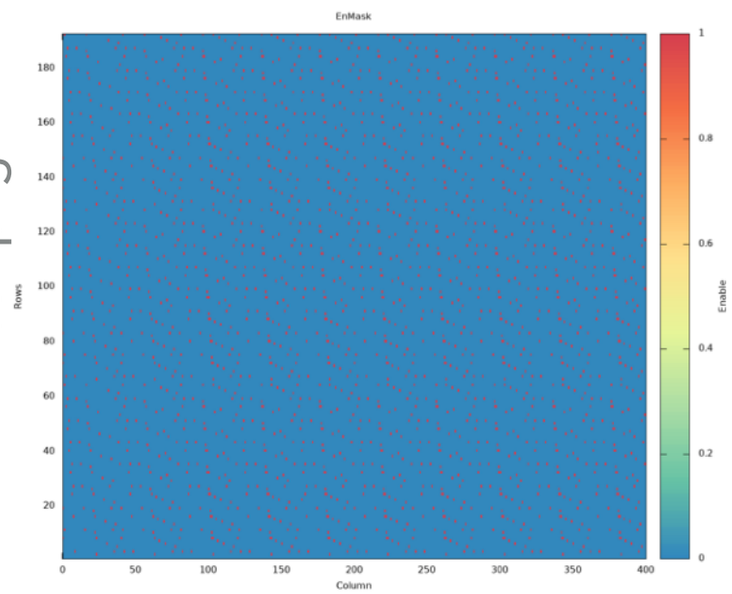
DIGITAL SCAN – 3 CHANNELS (THROUGH ADAPTER DUMMY SETUP)

- In the rd53a_test.json file, changed "OutputActiveLanes" to 7
- Changed the Trigger frequency in std_digitalscan.json file

Directly powered
VDDA: 1.186 V VDDD: 1.208 V

Trigger Frequency : 30 kHz

EnMask.png

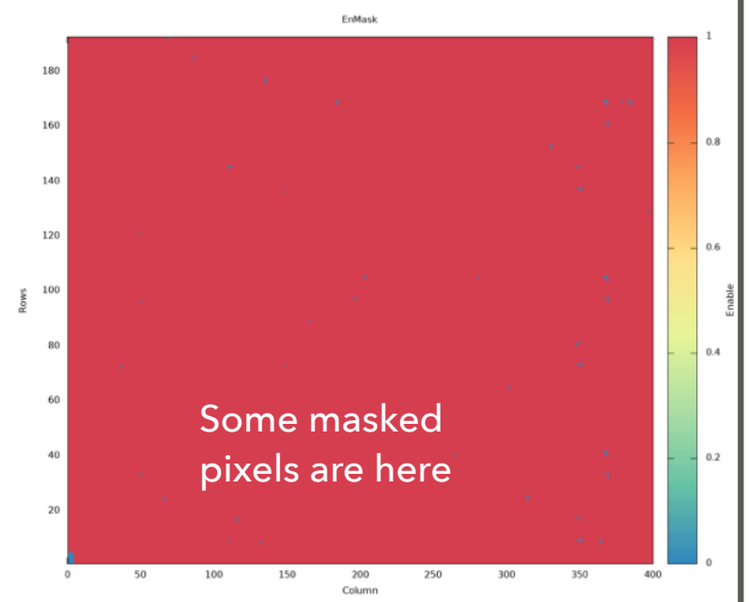


OccupancyMap.dat

```
 99 98 98 98 98 98 99 99 99 99 98 98 99 99 97 99 97
99 99 99 98 98 99 99 97 99 97 99 98 99 99 98 99 98
8 99 98 99 98 99 99 98 99 98 98 99 99 98 99 99 98 9
 99 98 98 99 99 98 99 99 98 99 99 98 98 98 99 98 98
99 98 99 99 98 98 98 99 98 98 98 99 98 98 98 98 98
9 98 98 98 99 98 98 98 98 98 99 99 99 99 98 98 99 9
 98 98 99 99 99 99 98 98 99 99 98 99 98 99 98 99 99
98 99 99 98 99 98 99 98 99 99 98 99 98 98 99 99 98
8 99 99 98 99 98 98 99 99 98
 98 98 99 98 99 98 98 99 98 98 99 98 100 98 99 98 9
 99 98 98 99 98 100 98 99 98 97 98 99 99 99 98 98 9
8 99 98 97 98 99 99 99 98 98 99 98 99 99 98 98 99 9
9 98 98 99 98 99 99 98 98 99 99 99 99 99 98 98 98 9
8 98 99 99 99 99 99 98 98 98 99 99 98 98 98 99 98 9
8 98 98 99 99 98 98 98 99 98 99 98 98 99 98 98 99 9
8 99 98 99 98 98 99 98 98 99 98 100 98 99 98 98 98
8 98 99 98 100 98 99 98 98 98 99 99 99 98 98 99 98
98 98 98 99 99 99 98 98 99 98 99 99 98 98
```

Trigger Frequency : 20 kHz

EnMask.png

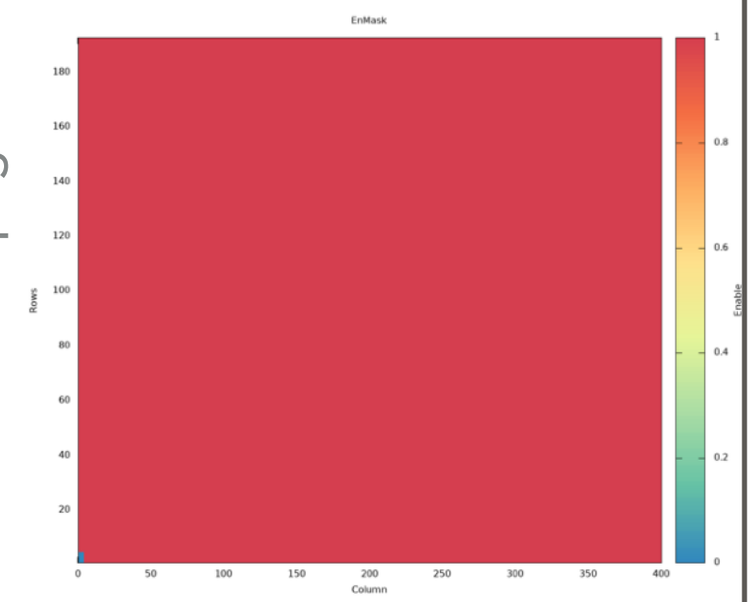


OccupancyMap.dat

```
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
```

Trigger Frequency : 18 kHz

EnMask.png



OccupancyMap.dat

```
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10

100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
```

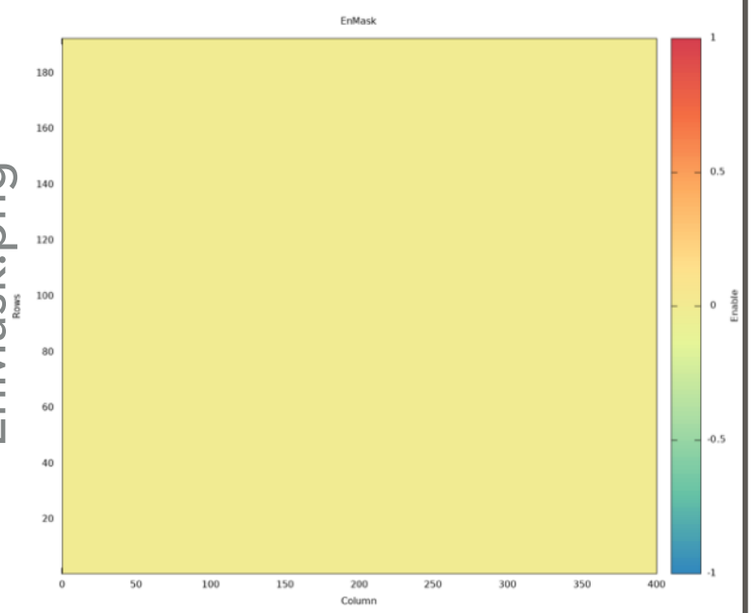
DIGITAL SCAN – 2 CHANNELS (THROUGH ADAPTER DUMMY SETUP)

- In the rd53a_test.json file, changed "OutputActiveLanes" to 3
- Changed the Trigger frequency in std_digitalscan.json file

Directly powered
VDDA: 1.186 V VDDD: 1.208 V

Trigger Frequency : 30 kHz

EnMask.png

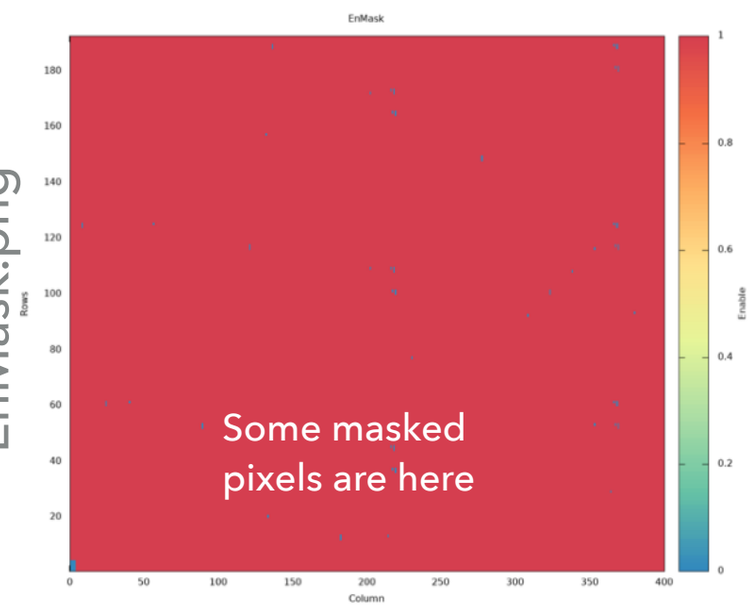


OccupancyMap.dat

```
 73 75 72 75 75 75 74 72 72 76 76 74 71 71 72 71 71
72 72 76 76 74 71 71 72 71 71 75 75 75 71 71 72 71
2 71 71 75 75 75 71 71 72 71 71 75 72 75 76 76 73 7
 72 71 71 75 72 75 76 76 73 72 71 71 75 72 73 77 74
76 73 72 71 71 75 72 73 77 74 75 73 75 72 75 75 75
3 77 74 75 73 75 72 75 75 75 74 72 72 76 76 74 71 7
 75 75 74 72 72 76 76 74 71 71 72 71 71 75 75 75 71
74 71 71 72 71 71 75 75 75 71 71 72 71 71 75 72 75
5 75 71 71 72 71 71 75 72 75
 75 76 73 74 74 75 73 72 71 72 73 71 74 72 75 72 71
72 71 72 73 71 74 72 75 72 71 72 75 75 72 71 71 75
5 72 71 72 75 75 72 71 71 75 71 75 75 71 71 71 74 7
 71 75 71 75 75 71 71 71 74 71 75 75 71 71 75 75 72
71 74 71 75 75 71 71 75 75 72 71 75 76 73 74 74 75
5 75 72 71 75 76 73 74 74 75 73 72 71 72 73 71 74 7
 74 75 73 72 71 72 73 71 74 72 75 72 71 72 75 75 72
71 74 72 75 72 71 72 75 75 72 71 71 75 71 75 75 71
5 75 72 71 71 75 71 75 75 71 71
```

Trigger Frequency : 18 kHz

EnMask.png

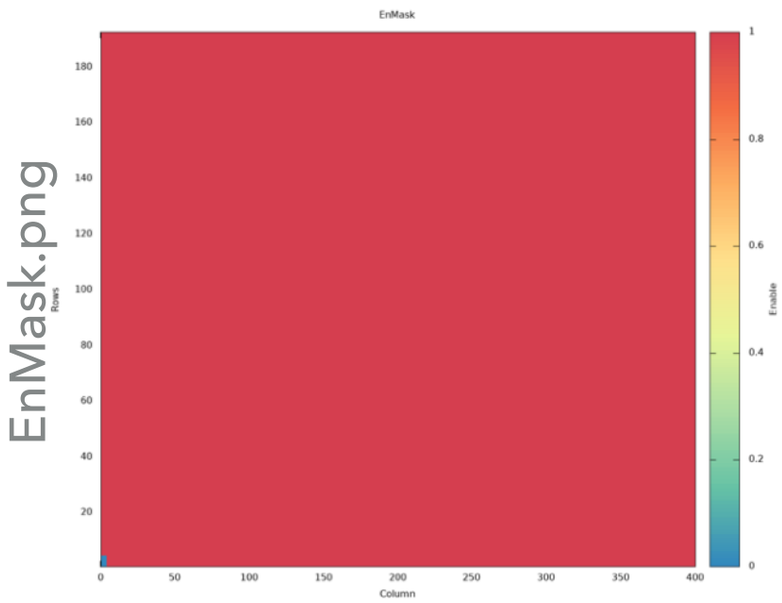


OccupancyMap.dat

```
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
```

Trigger Frequency : 15 kHz

EnMask.png



OccupancyMap.dat

```
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10

100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
```

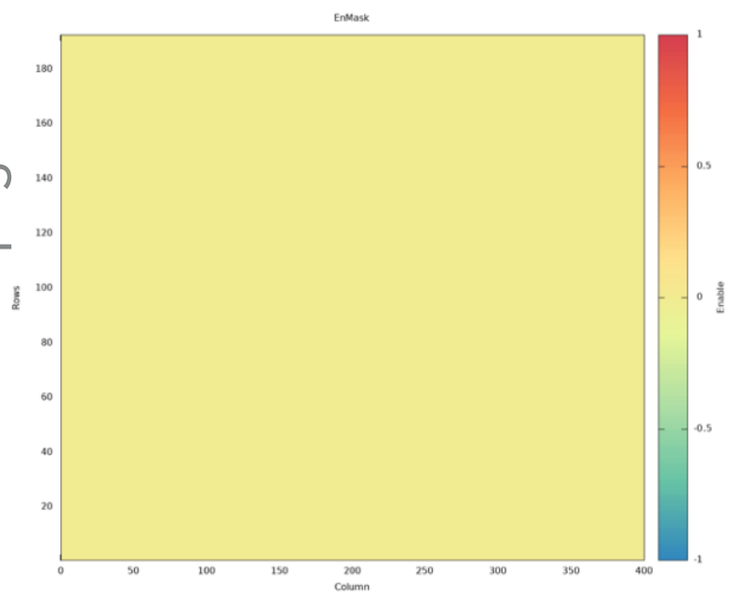
DIGITAL SCAN – 1 CHANNELS (THROUGH ADAPTER DUMMY SETUP)

- In the rd53a_test.json file, changed "OutputActiveLanes" to 1
- Changed the Trigger frequency in std_digitalscan.json file

Directly powered
VDDA: 1.186 V VDDD: 1.208 V

Trigger Frequency : 15 kHz

EnMask.png

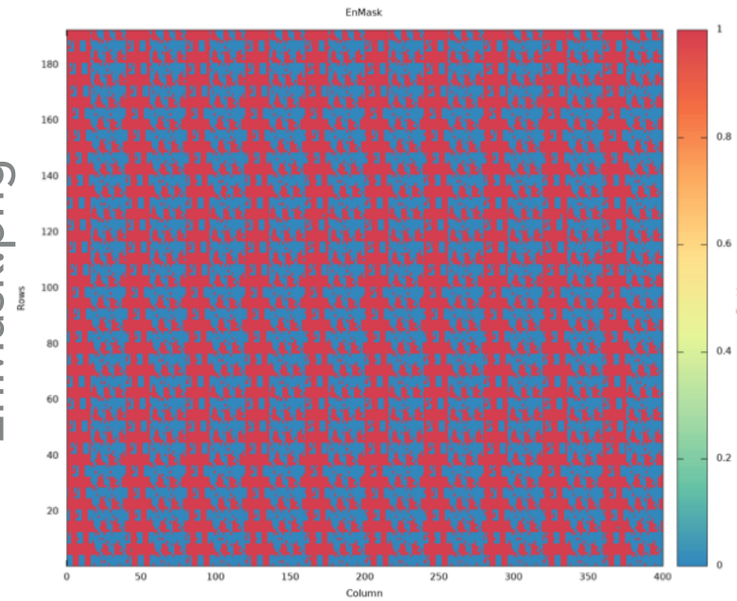


OccupancyMap.dat

```
0 80 83 81 78 78 78 78 84 80 82 83 78 79 79 82 80 8
 84 80 82 83 78 79 79 82 80 83 80 81 82 78 81 78 80
82 80 83 80 81 82 78 81 78 80 80 80 80 78 82 79 81
1 78 80 80 80 80 78 82 79 81 80 81 80 80 81 81 78 8
 79 81 80 81 80 80 81 81 78 82 80 80 83 81 78 78 78
81 78 82 80 80 83 81 78 78 78 78 84 80 82 83 78 79
8 78 78 78 84 80 82 83 78 79 79 82 80 83 80 81 82 7
 78 79 79 82 80 83 80 81 82 78 81 78 80 80 80 80 78
81 82 78 81 78 80 80 80 80
80 80 80 80 81 81 78 78 80 80 82 82 81 81 78 78 78
8 80 80 82 82 81 81 78 78 78 82 84 80 80 78 79 80 7
 78 78 82 84 80 80 78 79 80 78 80 80 82 81 81 81 78
79 80 78 80 80 82 81 81 81 78 82 80 80 80 81 82 84
1 81 78 82 80 80 80 81 82 84 79 80 80 80 80 81 81 7
 82 84 79 80 80 80 80 81 81 78 78 80 80 82 82 81 81
81 81 78 78 80 80 82 82 81 81 78 78 78 82 84 80 80
2 81 81 78 78 78 82 84 80 80 78 79 80 78 80 80 82 8
 80 80 78 79 80 78 80 80 82 81
```

Trigger Frequency : 12 kHz

EnMask.png

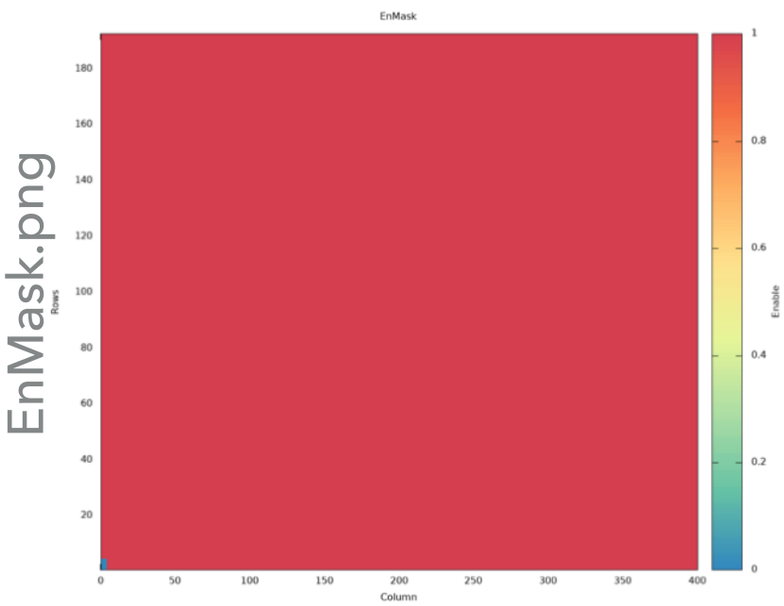


OccupancyMap.dat

```
8 98 100 100 100 100 99 98 100 98 99 99 99 99 98 98
0 100 100 99 98 100 98 99 99 99 99 98 98 98 98 100
9 98 100 98 99 99 99 99 98 98 98 98 100 99 99 99 98
 99 99 99 99 98 98 98 98 100 99 99 99 98 98 98 100
9 98 98 98 98 100 99 99 99 98 98 98 100 98 99 99 99
98 100 99 99 99 98 98 98 100 98 99 99 99 98 98 98 9
9 99 98 98 98 100 98 99 99 99 98 98 98 100 100 1
98 100 98 99 99 99 98 98 98 98 100 100 100 100 98 9
9 99 99 98 98 98 98 100 100 100 100 98 99 98 98 100

8 99 98 100 100 100 100 98 98 98 98 99 99 99 100 98
0 100 100 100 98 98 98 98 99 99 99 100 98 100 98 98
100 98 98 98 98 99 99 99 100 98 100 98 98 99 99 99
98 98 99 99 99 100 98 100 98 98 99 99 99 99 98 98 9
9 99 100 98 100 98 98 99 99 99 99 98 98 99 98 98 99
8 100 98 98 99 99 99 99 98 98 99 98 98 99 99 99 100
8 99 99 99 99 98 98 99 98 98 99 99 99 100 100 98 99
 99 98 98 99 98 98 99 99 99 100 100 98 99 100 100 1
```

Trigger Frequency : 10 kHz

EnMask.png

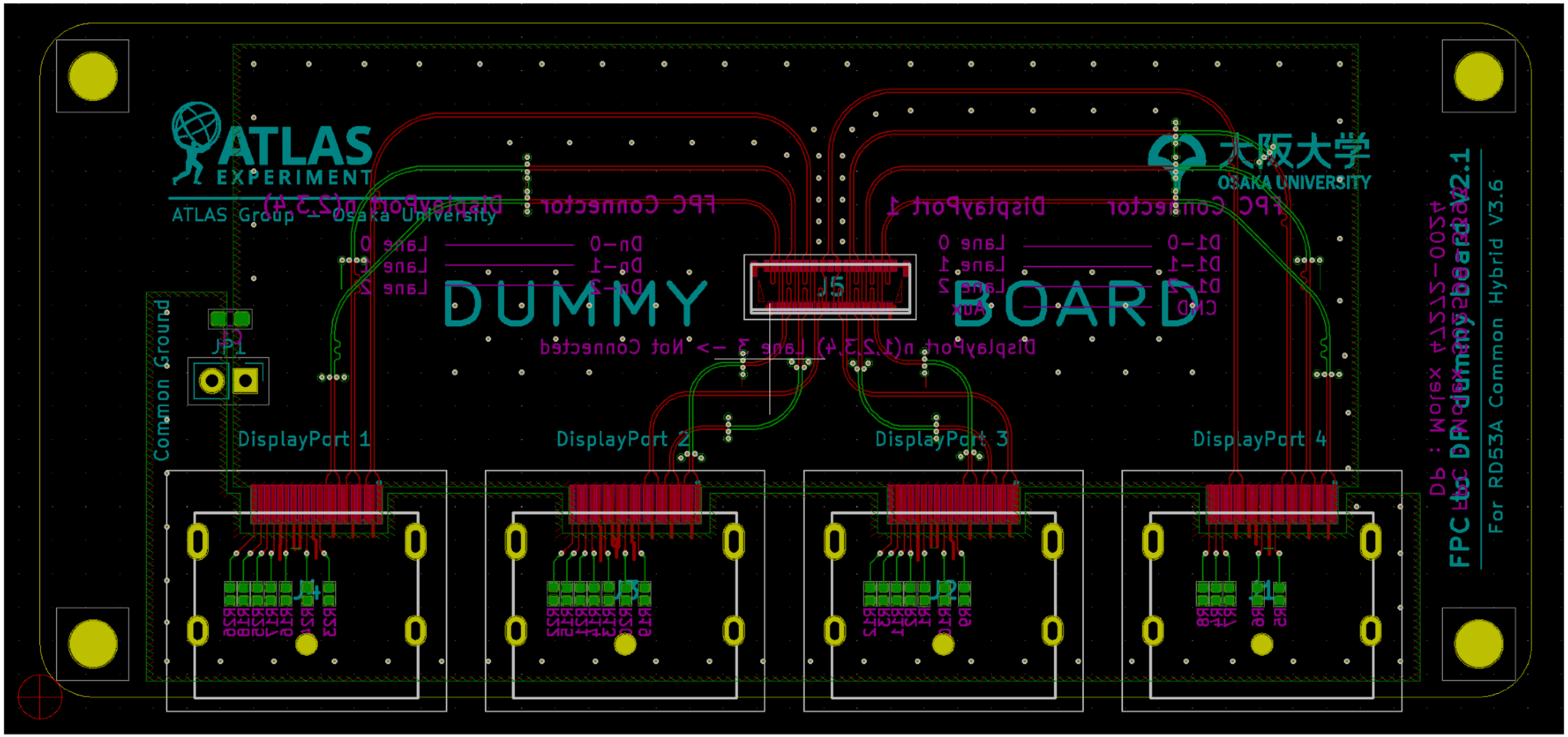


OccupancyMap.dat

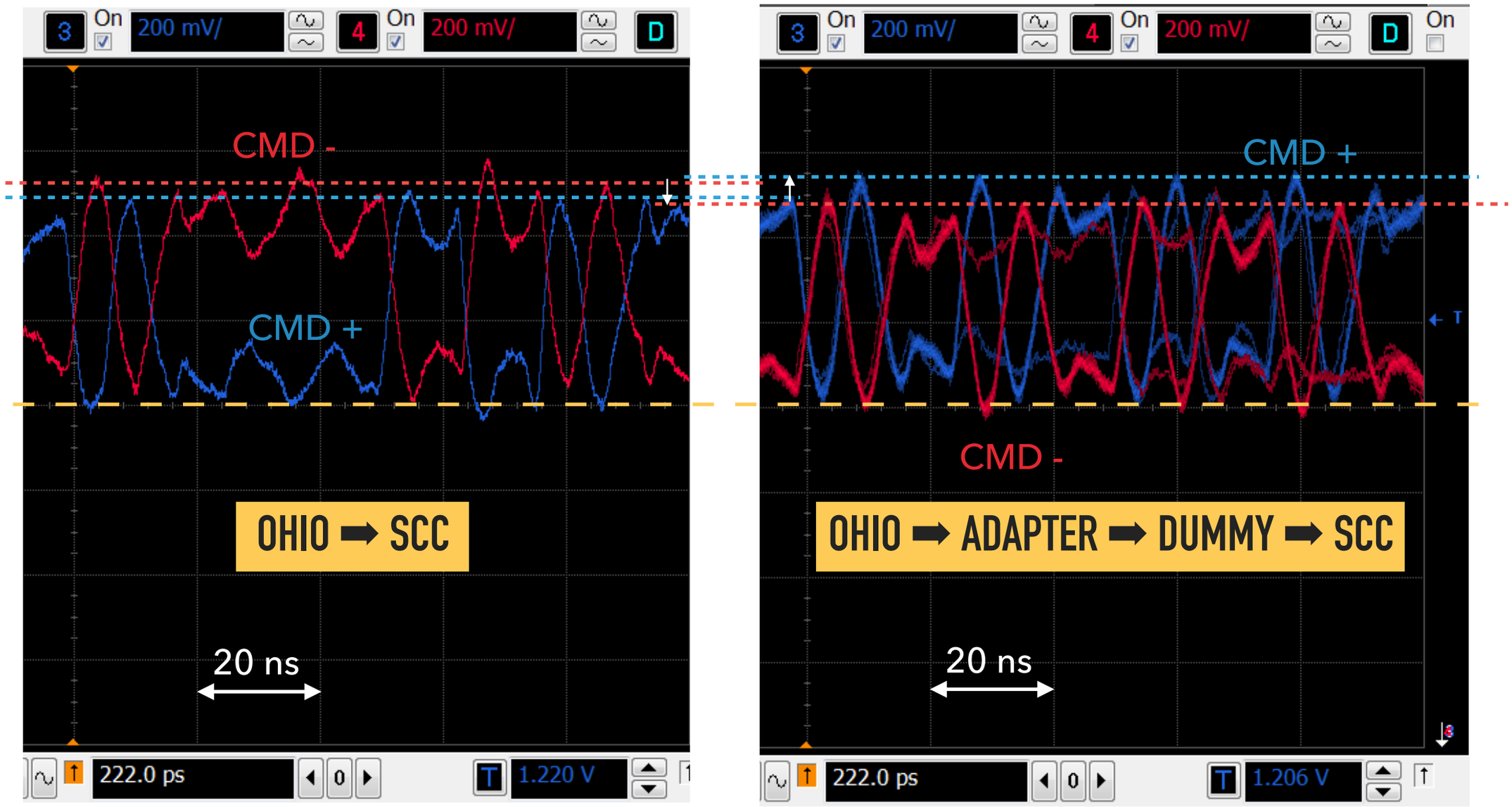
```
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10
00 100 100 100 100 100 100 100 100 100 100 100 100
 100 100 100 100 100 100 100 100 100 100 100 100 10

100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
100 100 100 100 100 100 100 100 100 100 100 100 100
0 100 100 100 100 100 100 100 100 100 100 100 100 1
```

DUMMY CARD VERSION 2.1

1. All lines are curved, but different in length.
2. Impedance controlled for via's (according to calculation).



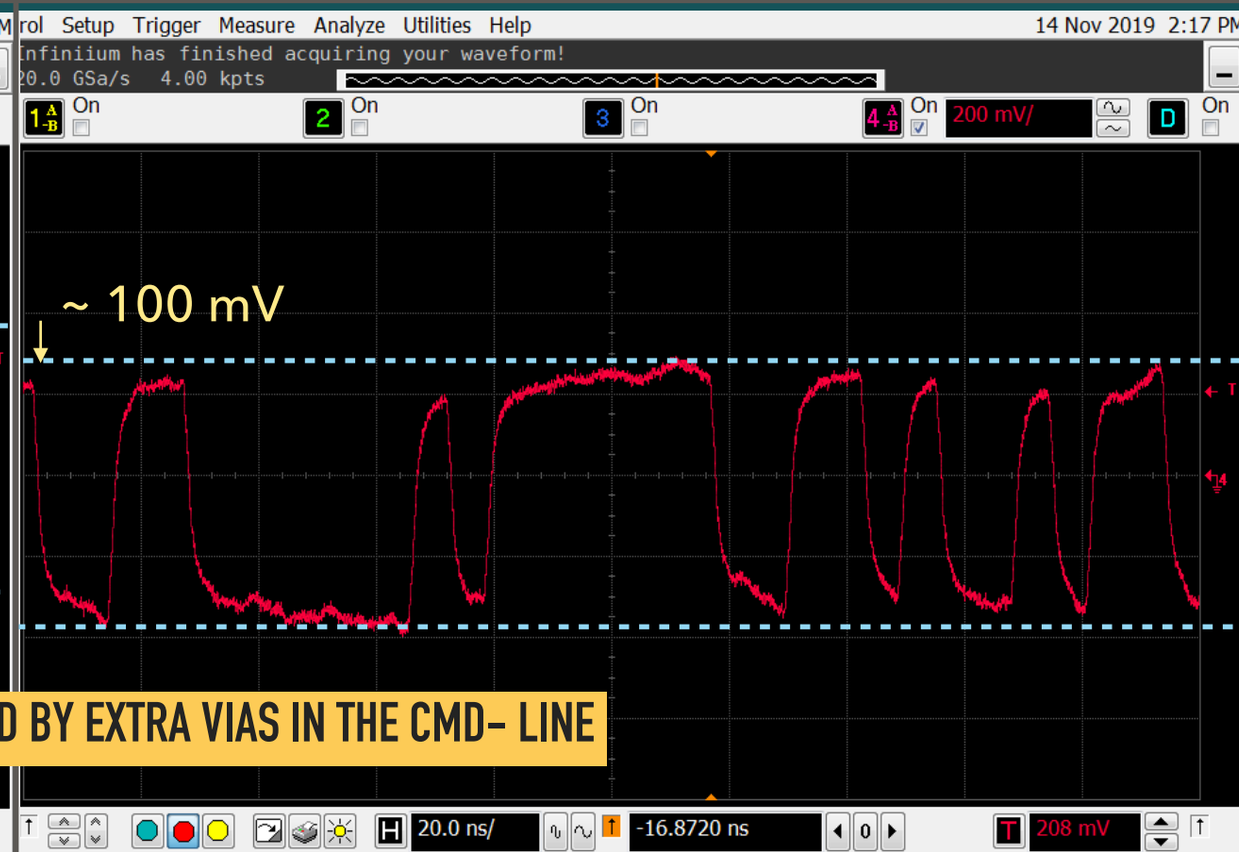
TESTING SIGNAL TRANSMISSION – CMD LINE



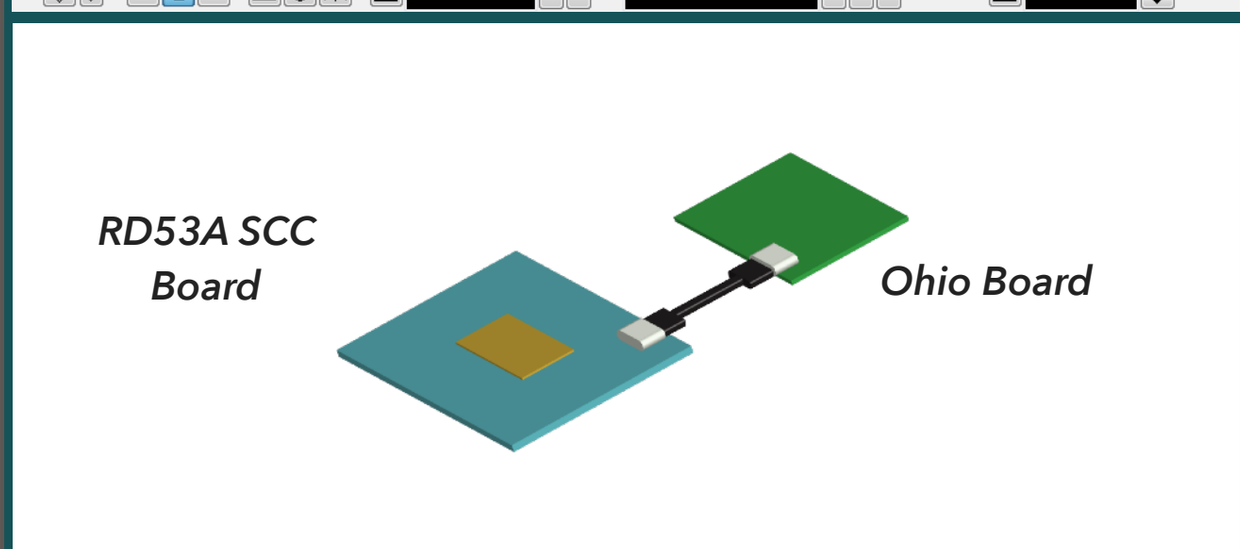
There is an offset of 1V

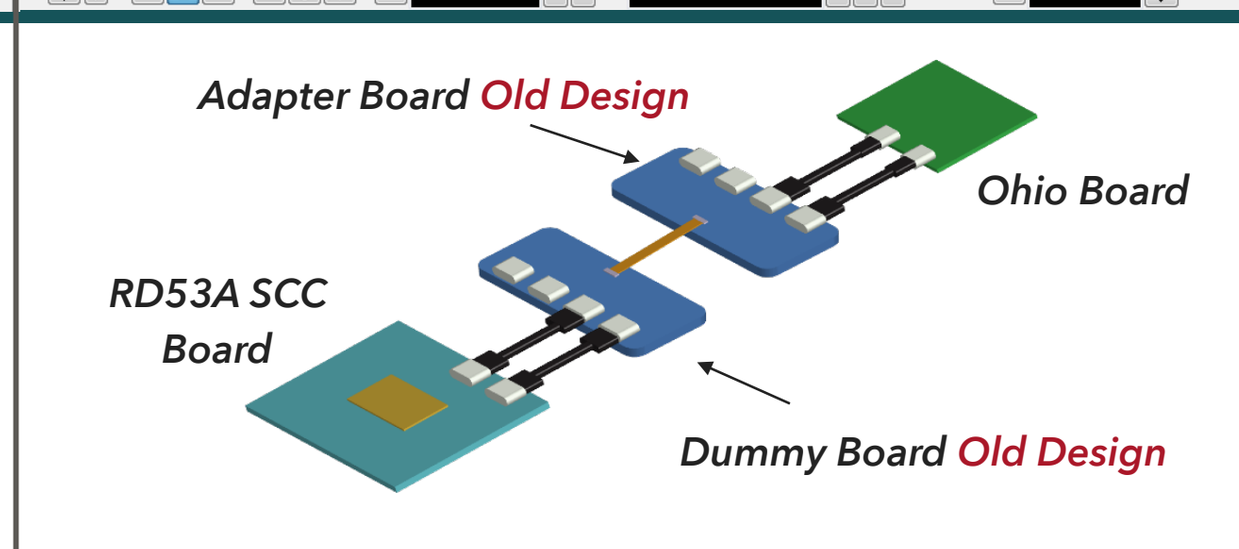
There are 4 more via's in the CMD- line compared to CMD+ line

COMPARISON – CMD LINE (DIFFERENTIAL)

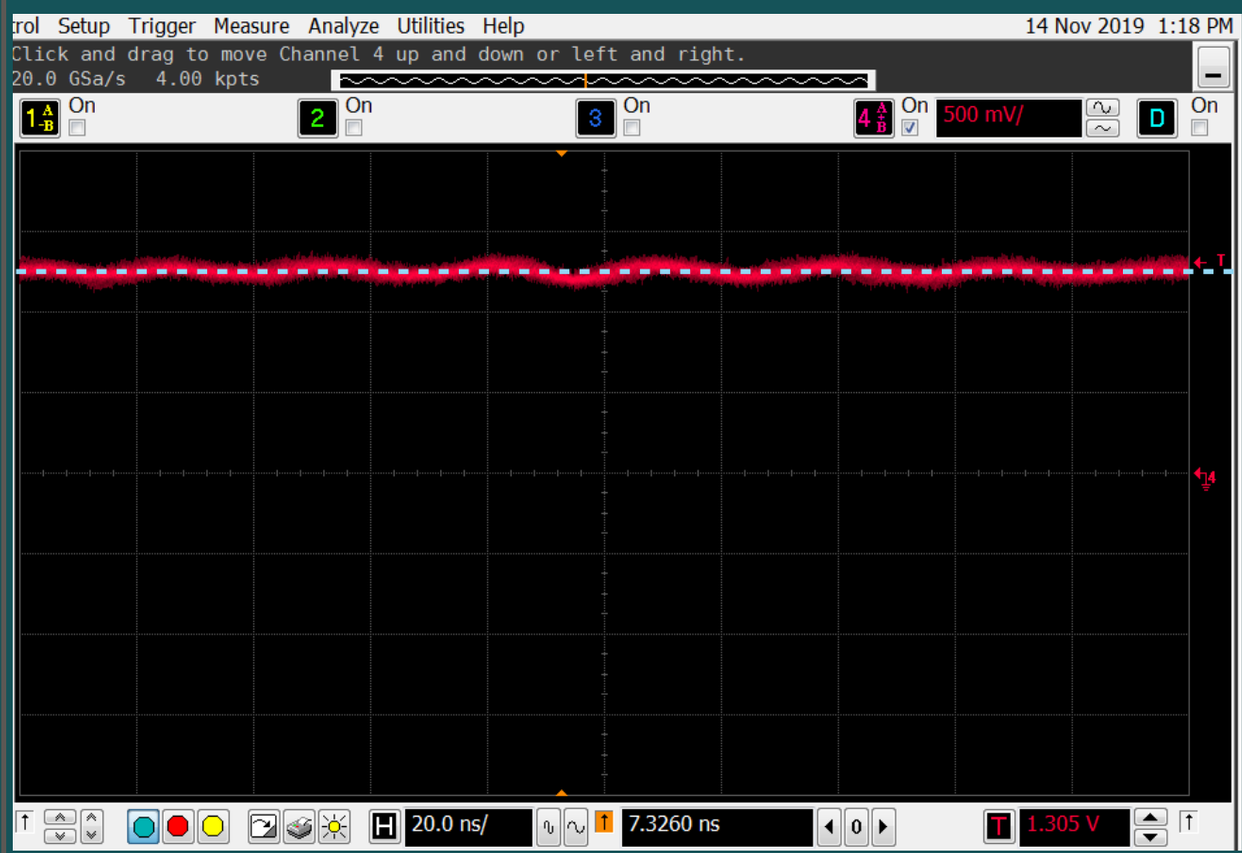


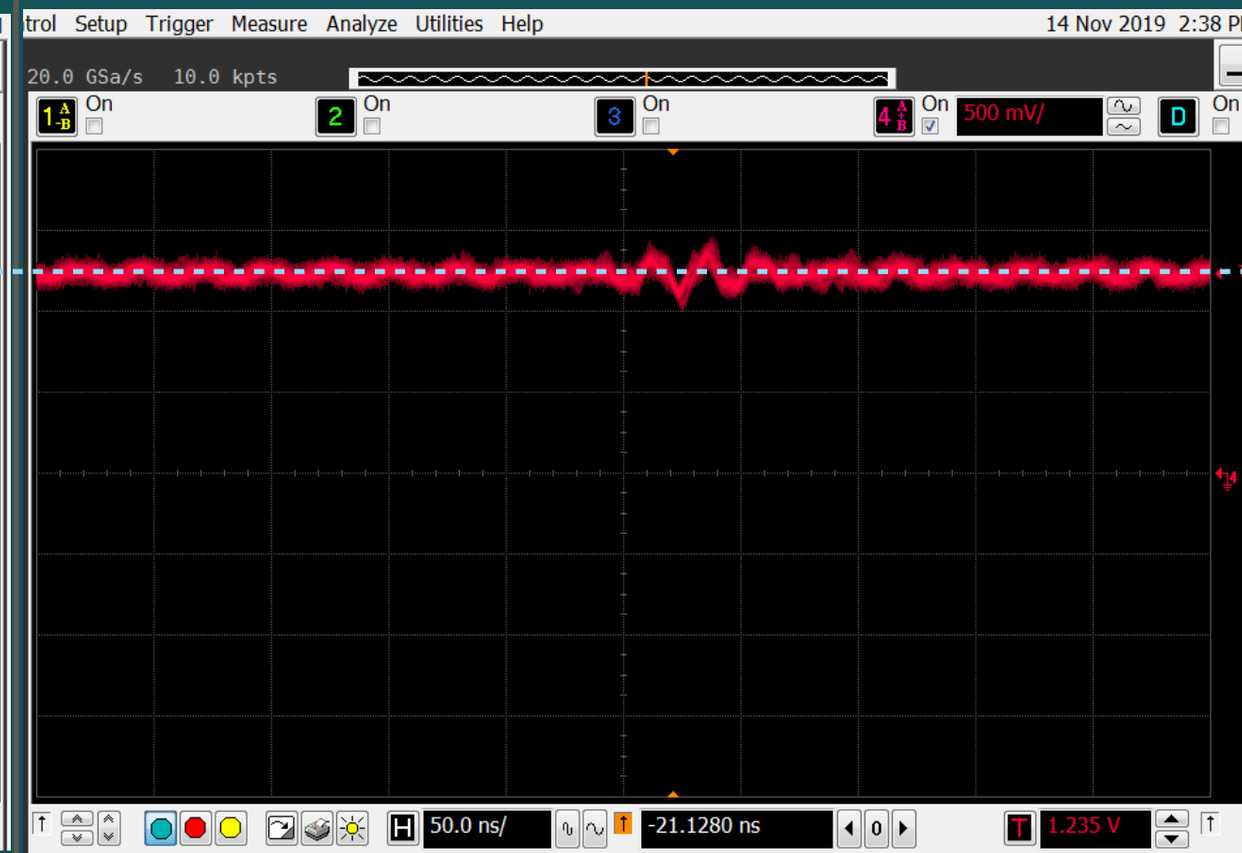
THE ISSUE IS LIKELY TO BE CAUSED BY EXTRA VIAS IN THE CMD- LINE

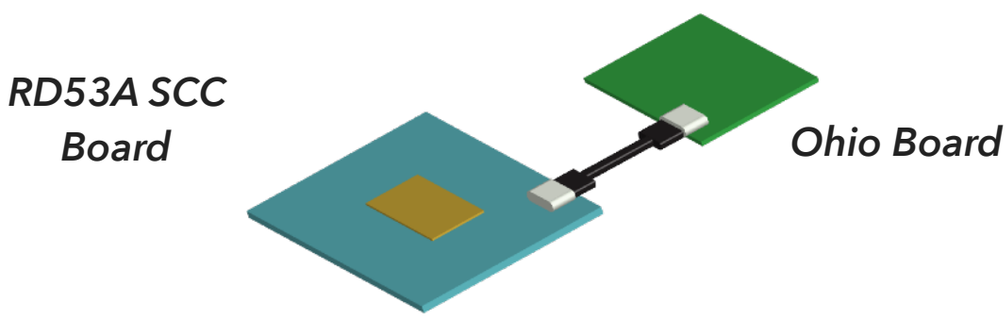


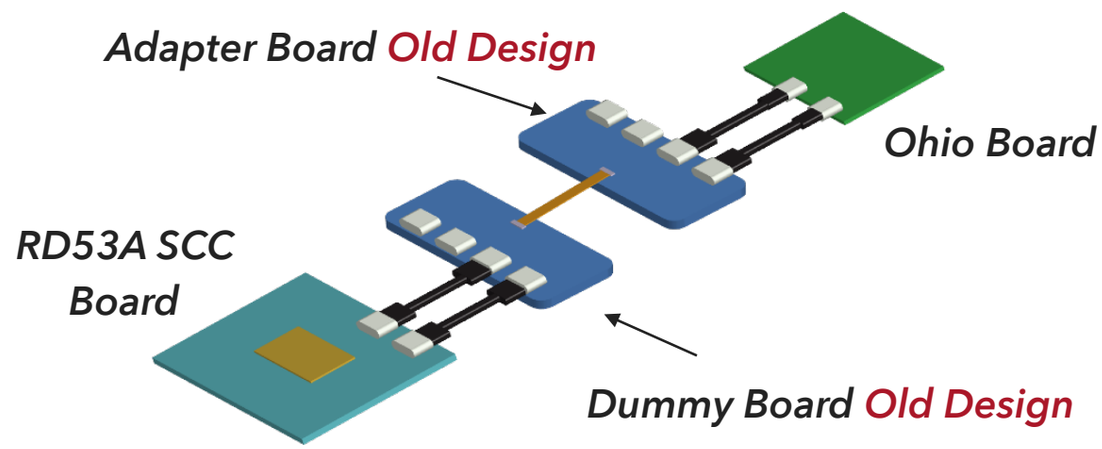


COMPARISON – CMD LINE (COMMON MODE)

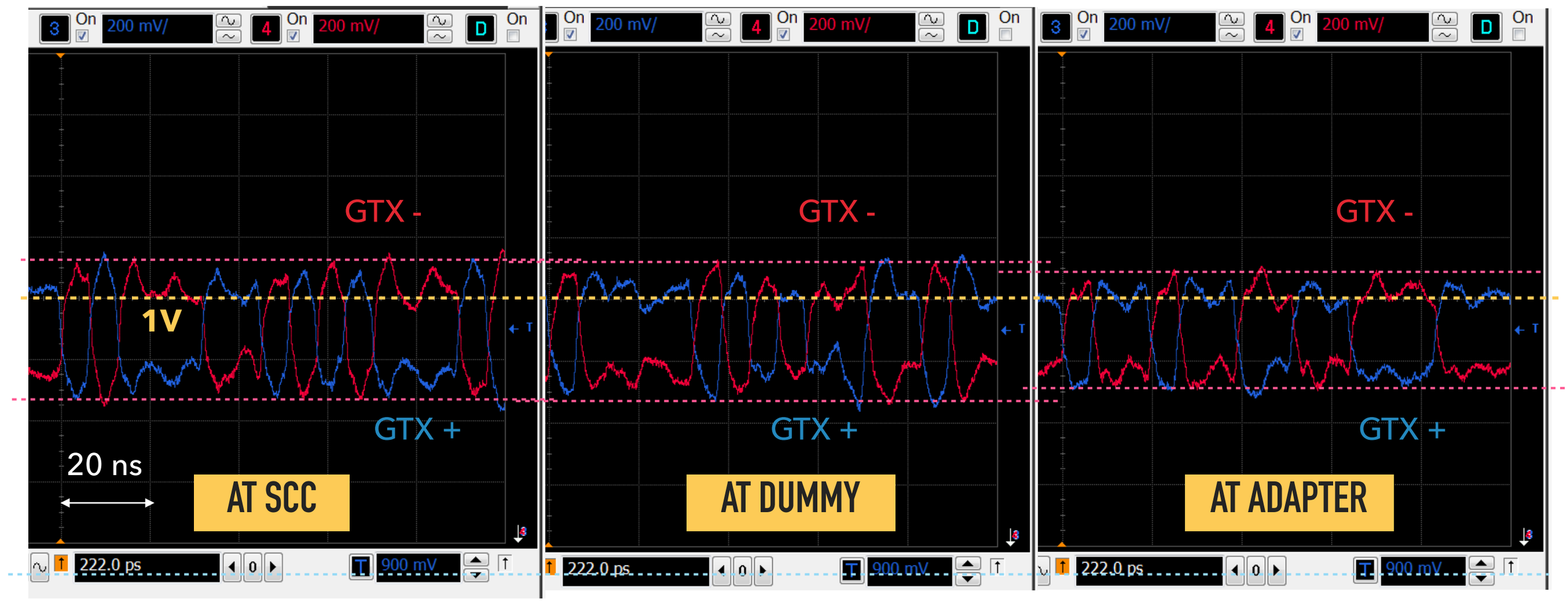


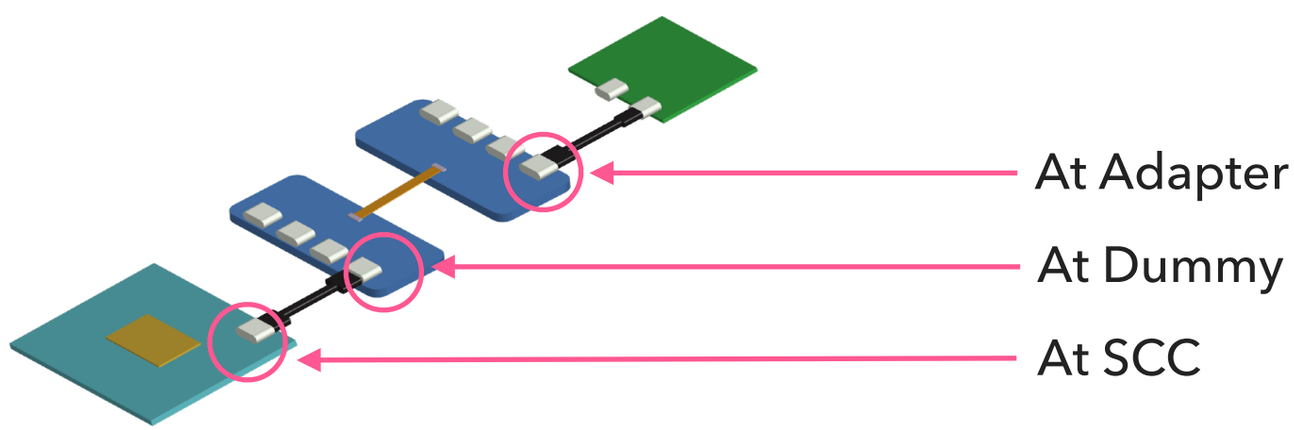






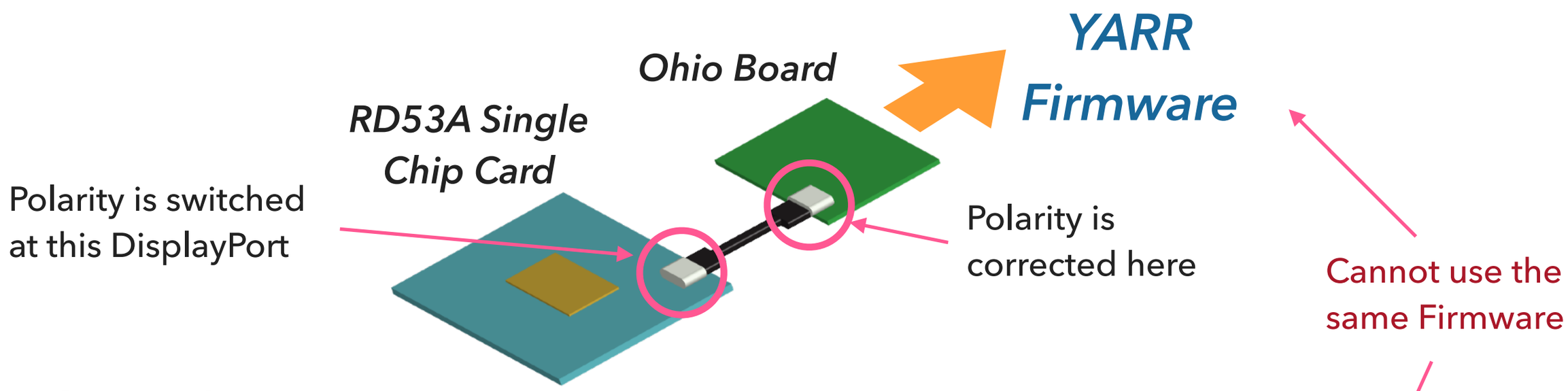
TESTING SIGNAL TRANSMISSION – GTX1 LINE





POLARITY FEATURE

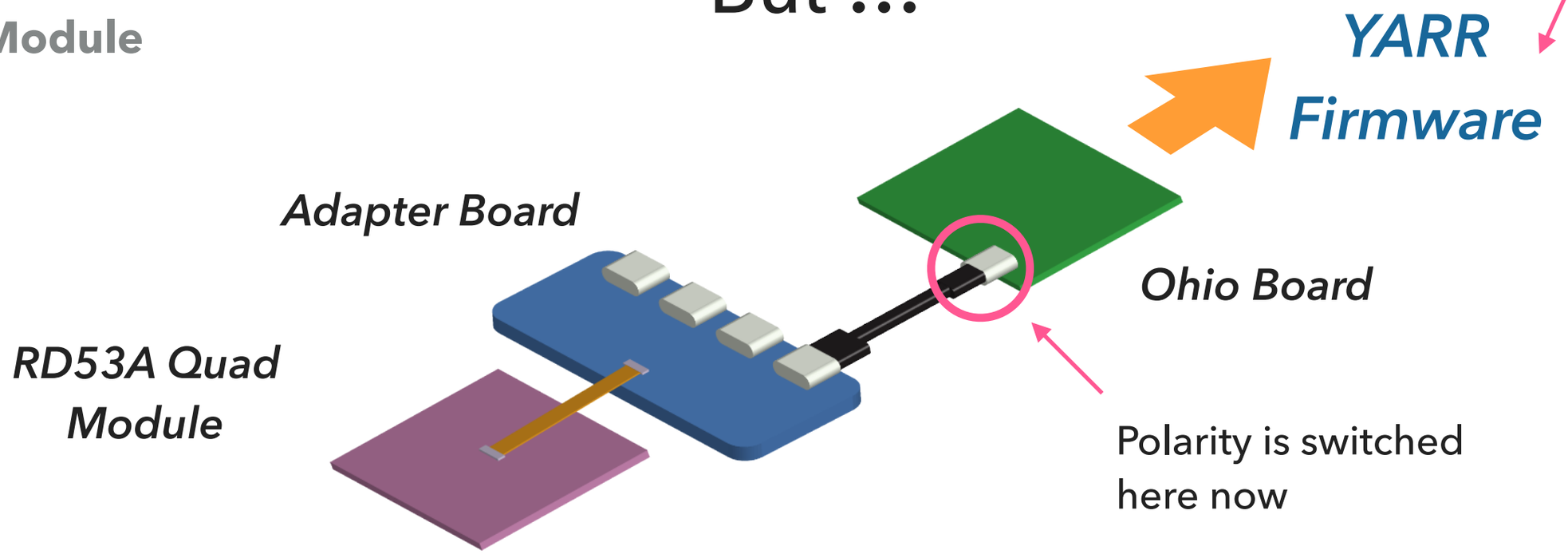
For a differential pair, P goes to N & N goes to P at the DisplayPort



Single Chip Card

But ...

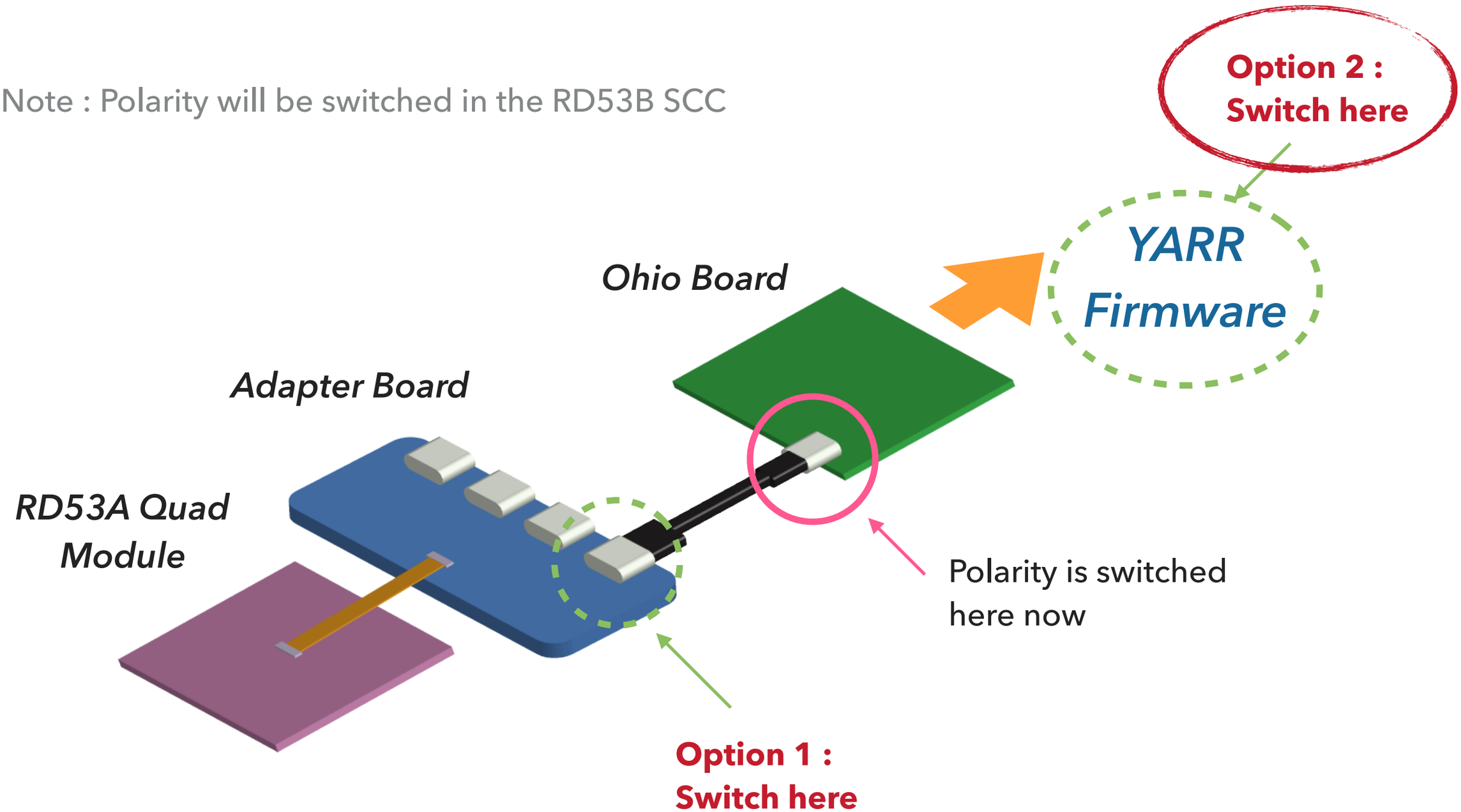
Quad Module



POLARITY FEATURE – SOLUTIONS

Decided on option 2

Note : Polarity will be switched in the RD53B SCC



ADAPTER BOARD – PIN MAPPING

ASIC			FPGA
Common Hybrid Notation	Lane		Lane
CMD_N	CMD N	↔	CMD P
CMD_P	CMD P	↔	CMD N
-	GTX 3 N	↔	GTX 3 P
-	GTX 3 P	↔	GTX 3 N
Dn2-	GTX 2 N	↔	GTX 2 P
Dn2+	GTX 2 P	↔	GTX 2 N
Dn1-	GTX 1 N	↔	GTX 1 P
Dn1+	GTX 1 P	↔	GTX 1 N
Dn0-	GTX 0 N	↔	GTX 0 P
Dn0+	GTX 0 P	↔	GTX 0 N
n=1,2,3,4			

DisplayPort ➡ Mini DisplayPort Cable

DisplayPort Source Connector				DisplayPort to Mini DP Cable Assembly			Mini DP Sink Connector		
Signal Type	Pin Name	Pin		Plug Pin		Plug Pin	Pin	Pin Name	Signal Type
GND	GND	2		2	↔	8	8	GND	GND
Out	ML_Lane 0 (p)	1		1	↔	12	12	ML_Lane 0 (p)	In
Out	ML_Lane 0 (n)	3		3	↔	10	10	ML_Lane 0 (n)	In
GND	GND	5		5	↔	13	13	GND	GND
Out	ML_Lane 1 (p)	4		4	↔	17	17	ML_Lane 1 (p)	In
Out	ML_Lane 1 (n)	6		6	↔	15	15	ML_Lane 1 (n)	In
GND	GND	8		8	↔	7	7	GND	GND
Out	ML_Lane 2 (p)	7		7	↔	11	11	ML_Lane 2 (p)	In
Out	ML_Lane 2 (n)	9		9	↔	9	9	ML_Lane 2 (n)	In
GND	GND	19		19	↔	19	19	GND	GND
In	Hot Plug Detect	18		18	↔	2	2	Hot Plug Detect	Out
CFG	CONFIG1	13		13	↔	4	4	CONFIG1	CFG
CFG	CONFIG2	14		14	↔	6	6	CONFIG2	CFG
GND	GND	11		11	↔	1	1	GND	GND
Out	ML_Lane 3 (p)	10		10	↔	5	5	ML_Lane 3 (p)	In
Out	ML_Lane 3 (n)	12		12	↔	3	3	ML_Lane 3 (n)	In
GND	GND	16		16	↔	14	14	GND	GND
I/O	AUX_CH (p)	15		15	↔	16	16	AUX_CH (p)	I/O
I/O	AUX_CH (n)	17		17	↔	18	18	AUX_CH (n)	I/O
PWR Out	DP_PWR	20		20	(no connection)	20	20	DP_PWR	PWR Out

Figure 2-10: DisplayPort to Mini DisplayPort Cable Connector Assembly Wiring

Compare the Green and Blue Columns

ASIC		Adapter DP Connector		Adapter DP Plug		Ohio Mini DP Plug		Ohio Mini DP Connector		FPGA
Common Hybrid Notation	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Pin	Lane	Lane
CMD_N	CMD N	17	CMD N	17	CMD N	18	CMD N	18	CMD N	CMD P
CMD_P	CMD P	15	CMD P	15	CMD P	16	CMD P	16	CMD P	CMD N
-	GTX 3 N	12	GTX 3 N	12	GTX 3 N	3	GTX 3 N	3	GTX 3 N	GTX 3 P
-	GTX 3 P	10	GTX 3 P	10	GTX 3 P	5	GTX 3 P	5	GTX 3 P	GTX 3 N
Dn2-	GTX 2 N	9	GTX 2 N	9	GTX 2 N	9	GTX 2 N	9	GTX 2 N	GTX 2 P
Dn2+	GTX 2 P	7	GTX 2 P	7	GTX 2 P	11	GTX 2 P	11	GTX 2 P	GTX 2 N
Dn1-	GTX 1 N	6	GTX 1 N	6	GTX 1 N	15	GTX 1 N	15	GTX 1 N	GTX 1 P
Dn1+	GTX 1 P	4	GTX 1 P	4	GTX 1 P	17	GTX 1 P	17	GTX 1 P	GTX 1 N
Dn0-	GTX 0 N	3	GTX 0 N	3	GTX 0 N	10	GTX 0 N	10	GTX 0 N	GTX 0 P
Dn0+	GTX 0 P	1	GTX 0 P	1	GTX 0 P	12	GTX 0 P	12	GTX 0 P	GTX 0 N
n=1,2,3,4		Source Side Pins		DisplayPort to Mini-DisplayPort Cable				Sink Side Pins		